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G. T. Flynn

An Electro Optical MTI System for the Detection of Artificial Satellites (the NITH Finder)

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FOR THE COMMANDER

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AN ELECTRO OPTICAL MTI SYSTEM FOR THE DETECTION OF ARTIFICIAL SATELLITES (THE NITH FINDER)

G. T. FLYNN

Group 94

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LEXINGTON MASSACHUSETTS

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1.0 INTRODUCTION

This note describes a video disc recorder and a companion processor which have been built to automatically detect faint satellites in deep space. The purpose of the system is to eliminate the need for a trained dedicated observer. While it is anticipated that the probability of detection on any search will be on the same order as an observer, there are several important advantages over a manual system:

1. The automated process is not subject to fatigue.
2. The time to detection is faster.
3. Automatic handoff to a computer of satellite position and velocity is possible.
4. Generation of an accurate located video gate for SOI and/or tracking is available.

It is not purported that this system is an optimum design in terms of scan coverage rates or processing techniques; it represents the best approach for a reliable design that could be implemented using a conservative estimate of available technology. The system is completely compatible with standard 525 lines, 30 frame/sec television scan rates. It is therefore completely compatible with the rest of the GEODSS site equipment.

1.1 VELOCITY FILTER MTI

If the telescope is placed in a sidereal track, stars which are essentially at infinity remain stationary within the field of view, whereas satellites move with respect to this stationary background. If successive frames are recorded and played back some time later to provide

a delay such that a satellite will be displaced one or more resolution cells, a simple velocity filter may be implemented as shown in Figure 1.

In order to provide a continuous output from the record playback mechanism, a set of four moving (stepped) heads are used. One is recording, one playing back and two retracing. The heads are stepped from the outermost track on a 16" disc for a maximum of 64 tracks inward. The stepping takes place during the vertical retrace interval and both record and playback are implemented with the heads stepping in the same direction to minimize track misregistration due to mechanical backlash. Since it takes the same time to retrace the heads to the first record track as it did to reach the last track, the maximum delay between input video and played back video is 2 x 64 or 128 frames. This choice of delay (T_{MAX}) as a maximum is based on requirements dictated by the system parameters, i.e., FOV (Field of View); α (Sensor Resolution Cell Size); ω (Satellite Velocity); and equalization limits for changing track radii. Figure 2 shows the minimum time delay required before subtraction takes place versus satellite velocity. The absolute minimum time delay available is a single frame. The choice of time delay is selectable in 0.1 second increments by means of thumbwheel switches on the master control panel. A choice of "zero" delay yields a one frame delay and any selection of delay beyond the maximum causes the machine to cycle between the outer and inner limit switches on the disc which provides a delay slightly greater than 128 frames, but uncalibrated.

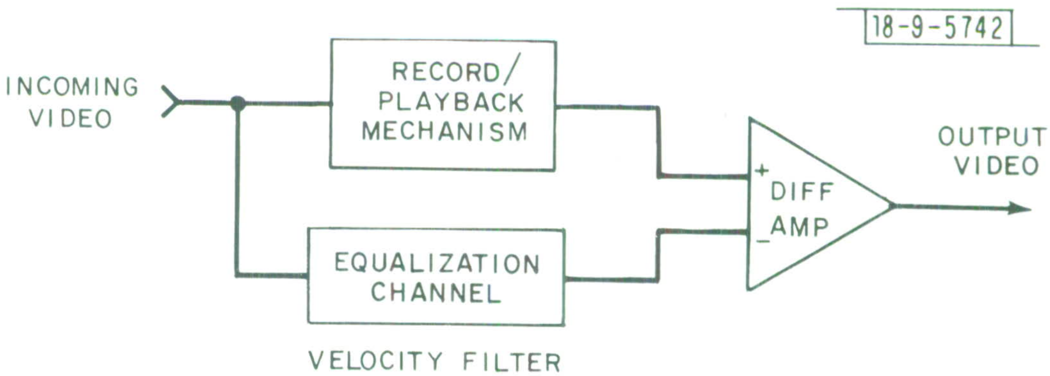

Fig. 1. MTI velocity filter diagram.

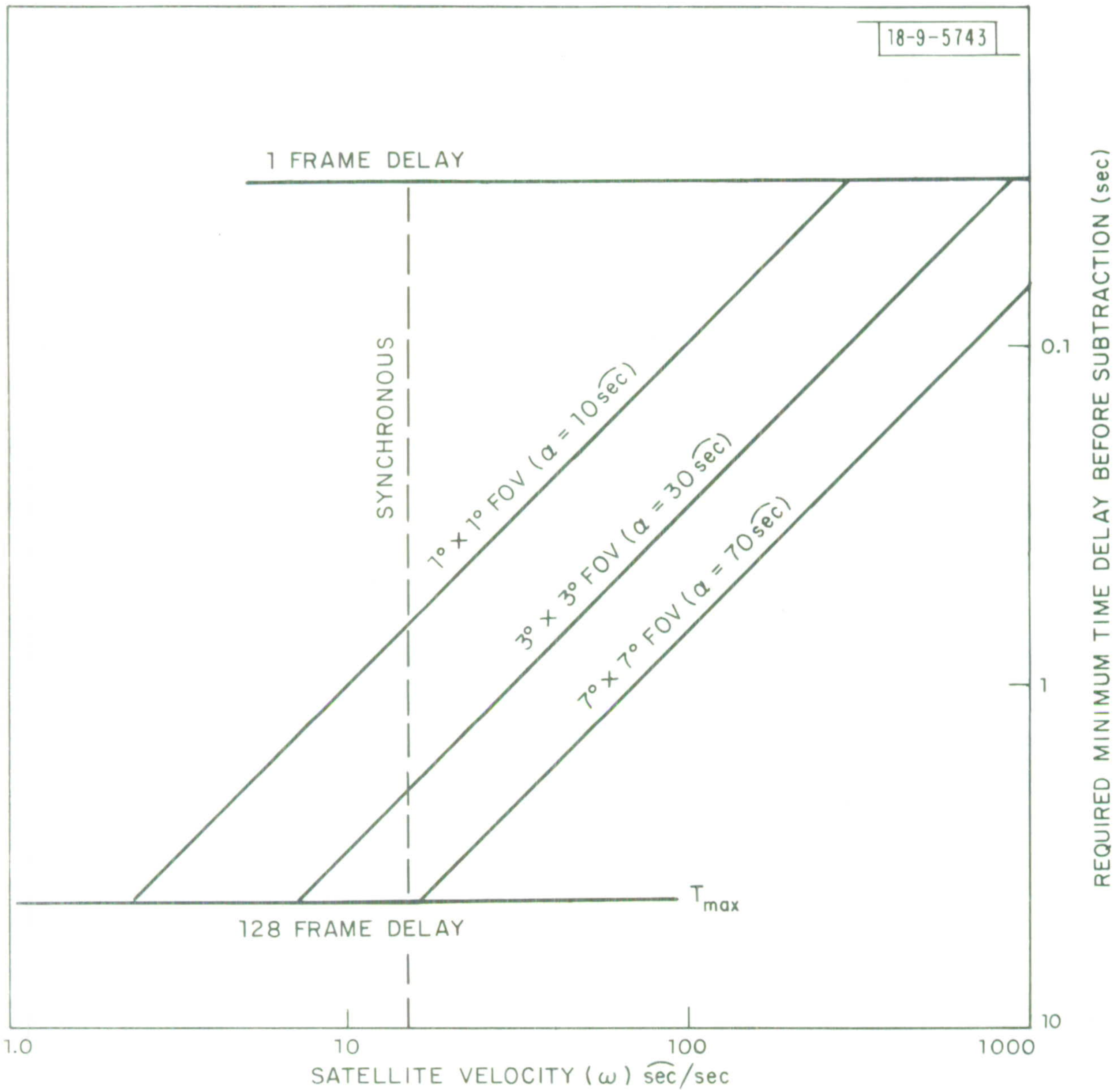

Fig. 2. Angular velocity (ω) vs required difference delay.

The equalization problem is discussed in some detail in the final report on the Video Disc Processor (see Westinghouse Final Report BB-284) and will not be covered in depth here. However, it is necessary to understand that in order for this system to operate, it is necessary for the played back video to be a "high fidelity" replica of the incoming video. Any distortion will result in a "residue" of clutter after subtraction.

In order to minimize the residue, several steps have been taken. Incoming video is modulated and demodulated to insure that any non-linearity inflicted on the delayed video is also inflicted on the "live" video. This also allows for fine delay equalization of the live video to insure registration. A clock track recorded on the disc provides a "hard lock" synchronization for the camera. This same clock track is servo loop controlled against a crystal clock reference to insure that the disc rotational velocity is held constant.

Of the possible problems, edge effects are the most serious. Typically, the sort of background that is encountered are bright stars which provide an abrupt transition from a fairly homogeneous night sky background to peak white level. Even a slight misregistration between subtracted frames will cause a significant residue which could defeat any automatic detection scheme. Figure 3 shows the result of the subtraction of two images, the video levels go from black to peak white in 200 nanoseconds and the positional error between the two waveforms is 100 nanoseconds or less than 1/2 of a resolution cell. The result after

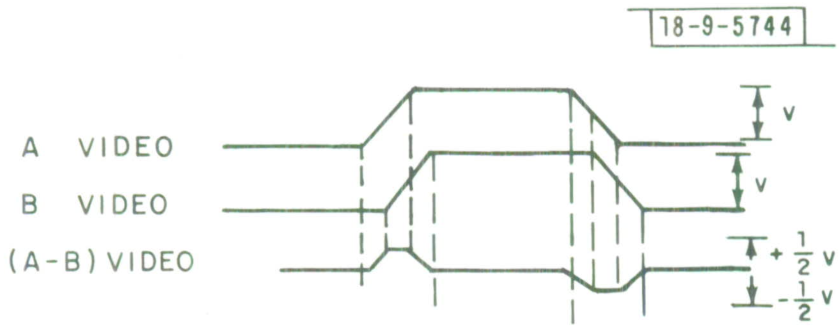

Fig. 3. Pictorial representation of timing errors.

differencing is the (A-B) video waveform which is the two 100 nanosecond pulses shown. Low pass filtering after differencing will further reduce the amplitude of these pulses, but will not eliminate them.

Some misregistration error is unavoidable; "seeing" conditions, i.e., atmospheric effects, will cause star images to wander as much as 40 nanoseconds in a 1° FOV; time base instability and head motion will add about another 40 to 50 nanoseconds.

Additional edge residues can be caused by unequal phase and frequency response characteristics in the two subtracted channels. For example, if a pulse is fed to two low pass filters with slightly different time delays and transient responses, the subtraction of those channels will yield a transient residue that cannot be eliminated by either amplitude or time delay adjustments. In the recording process, the video signal is transformed to a frequency modulated carrier (constant pulse width, variable frequency) and hard limited before recording. Normally, the demodulation consists of a hard limiting amplifier followed by a discriminator and low pass filter. The bandwidth of the recording track varies slightly from the outermost to innermost track because of the increased recording density on the inner tracks. By limiting the head travel to 64 tracks, this effect is minimal. Further, by subtracting the two pulse trains before low pass filtering, the most serious effects of transient response mismatch are avoided.

The bandwidth of the record track is an important factor in determining the ultimate signal to noise ratio achievable and great care has been

taken to achieve the maximum bandwidth possible by very careful head design to minimize the head gap width. Likewise, the magnetic material for the disc and the coating of the disc have been carefully selected to optimize signal to noise and bandwidth in the recording process.

One more important step that has been taken is to strip the sync and blanking from the video prior to recording. In this way, the slope of the FM deviation for the video is approximately double that which would be achievable if the sync were carried along. This corresponds to a 6dB improvement in achievable signal to noise ratio. Since the disc rotational velocity is hard locked to the sync track, the sync information contained on the video is redundant and may be reinserted after demodulation and low pass filtering.

Figure 4 is a more complete diagram of the differencing processor.

1.2 VIDEO AGC - (AUTOMATIC GAIN CONTROL)

One of the more important assumptions regarding overall system performance is the fact that the sensor (camera) is photon noise limited. That is, the noise contribution from the night sky background radiation is much greater than all the sources of instrument noise. This insures that the system is operating at the maximum possible sensitivity within the dynamic range limitations of the system.

Because the noise level of the disc is higher than the camera noise level, some video processing is required to maintain a photon noise limited signal through the record/playback process. The technique for implementing this is to amplify the video signal before recording and

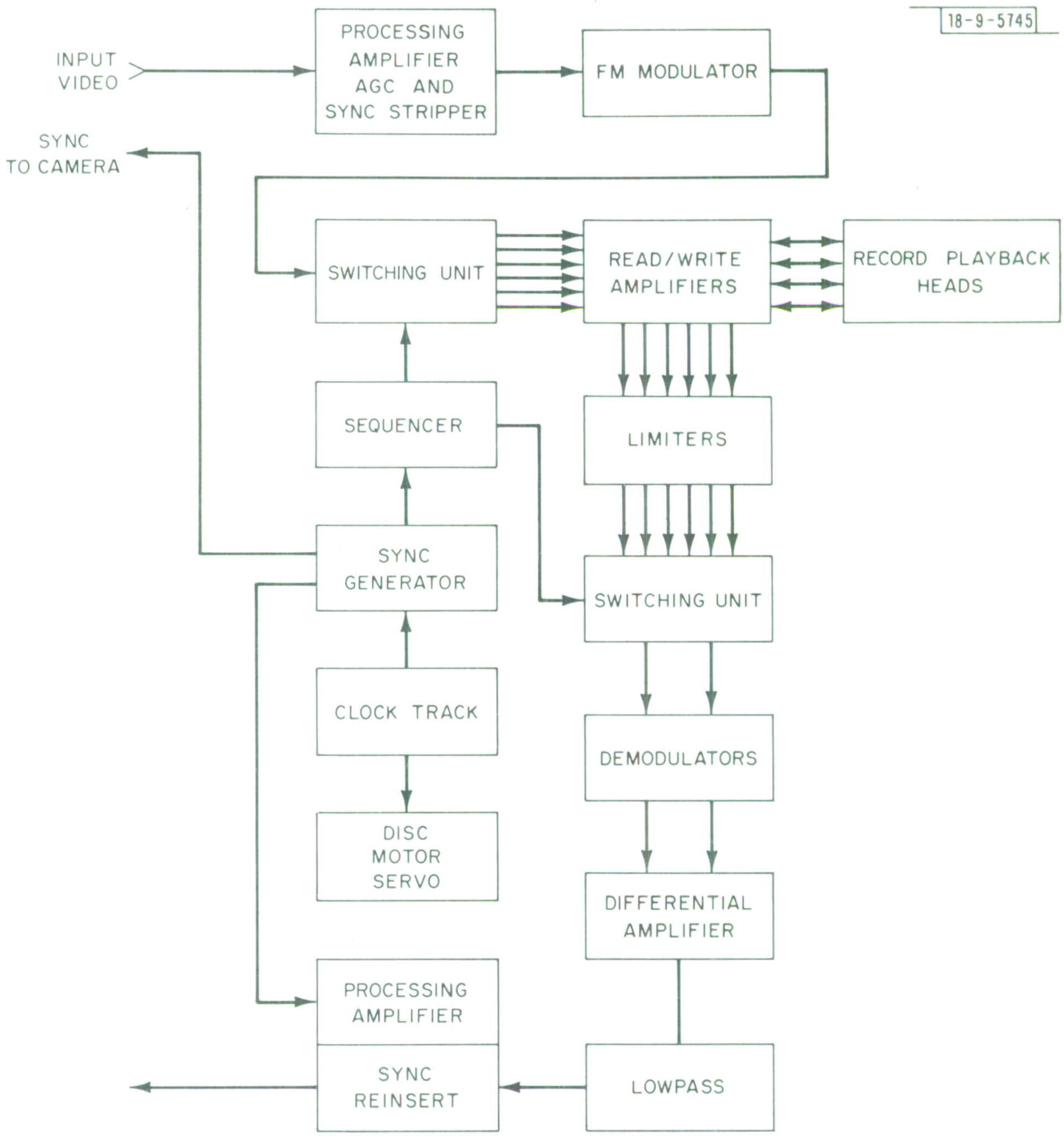

Fig. 4. Block diagram of video disc processor minus integrator.

clip the peak white level of bright stars. This process when implemented in an AGC system maintains a constant ratio of RMS background to peak white signal level.

A fair approximation of the RMS background noise may be obtained by high pass filtering the video and detection of the resultant. This resultant voltage is moderately effected by scene changes, i.e., the density of bright stars. However, this scene sensitivity is not serious enough to prevent adequate tracking of the noise. The most serious limitation is the amplification of the video pedestal particularly with large shading effects.

In order to limit the pedestal amplification, the AGC amplifier has been designed with a flat frequency response at unity gain and high frequency boast at maximum gain. This tends to differentiate bright stars or satellites, but does maintain a reasonably constant pedestal level.

1.3 VIDEO DIFFERENCE

Before proceeding with a discussion of the rest of the system, a few words are in order by way of comparison of the performance of this system to the so called maximum likelihood detection schemes. The ideal maximum likelihood detector will find the mean value of background in each resolution cell and store that value as a calibration. If the background is Poisson distributed, both the mean and the variance can be estimated from the same calibration. Because more than one sample is required for a good calibration estimate, either many samples of the

same cell must be taken or the background may be considered homogeneous and the average of an ensemble of adjacent cells (usually the entire FOV) would be used to determine the mean value of background which would be the same for all cells in FOV. On the basis of this mean value, a threshold may be set which would yield a fixed false alarm rate and a probability of detection curve corresponding to S/N. While in principle this is an ideal detector, in practice it does not take into account the very serious problems of variation in background across the FOV due to such effects as astronomical clusters of high intensity background, variations due to weather (clouds), vignetting in the telescope, X-Y shading of the sensor and target blemishes in the sensor.

In one respect the difference process is very similar to the maximum likelihood process. The mean value of the background is subtracted on an element by element basis, thus establishing the mean value at zero regardless of the background variation or what caused it. This is a very important step in any practical detection scheme which must use real world hardware rather than idealistic models.

Consider a variation in the mean value of background of ΔB across the FOV; the variation in the deviation of the background would be $\sqrt{\Delta B}$. Assuming that the threshold would be set somewhere in the tails of the distribution for an acceptable false alarm rate on the basis of the mean value of background, the threshold setting could be in error by an amount approaching $2\Delta B$ somewhere in the FOV. Since the false alarm rates change rather drastically in the tails of the distribution a

rather small value of ΔB could be catastrophic, driving the overall false alarm rate far beyond any acceptable limit.

For example, consider a background level of 100 photoelectrons and a variation in that background of ±10 percent due to shading. Figure 5 shows graphically the effect this variation causes in the number of threshold crossings as a function of X, Y position.

For the values chosen, the variation in background is equal to one standard deviation. Thus, if the threshold were nominally set for a P_{fA} of 10^{-9} the P_{fA} would vary from 10^{-6} to 10^{-12} due to shading alone. On the other hand, the change in the standard deviation is negligible. Therefore, by subtracting out the mean value of background, the standard deviation becomes:

$$\sqrt{2(B \pm \Delta B)}$$

For the values given it would be a range from 13.4 to 14.8 with a threshold setting for a nominal P_{fA} of 10^{-9}, i.e., $\sigma = 6$, the error from the optimum threshold setting across the FOV would be ±0.36.

It should be clear from this discussion that the threshold should not be set on the basis of the mean background level, but on the maximum acceptable false alarm rate, and that the mean value of the background should be removed prior to detection. Further discussion of the detection technique will be covered in Section 2 dealing with the automatic detection system.

1.4 POST DIFFERENCE INTEGRATION

There are several places in the overall system where integration may be performed to increase signal to noise ratio. The most obvious and often suggested is at the photocathode of the sensor. It has been shown[1] that photocathode integration adjusted to match the dwell time of the satellite in a resolution cell (α/ω) will enhance the effective S/N directly proportional to (T) the integration time.

The next place in the system that integration may be implemented is before differencing and the gain is proportional to $\sqrt{n}$ where n is the number of frames integrated. Finally, the last place that integration may be performed is after differencing and the gain again would be proportional to $\sqrt{n}$. From this it would seem as though that there is no particular advantage in the particular location of the integrator, and if the recording process were noiseless this would be true. The instrument noise level of the recorder is quite low, approximately 36 to 39dB* below peak white. If the input S/N into the recorder is low, i.e., 6 to 10dB, the degradation due to the recording process is negligible. The output signal to noise is given by:

$$\frac{S_o}{N_o} = \frac{S_{in}}{\sqrt{N_{in}^2 + N_R^2}}$$

where

*When expressed in dB S/N always means $20\log\frac{\text{P-P SIGNAL}}{\text{RMS NOISE}}$ unless otherwise stated.

S_o = Signal out

N_o = Noise out (RMS)

S_{in} = Signal in

N_{in} = Noise in (RMS)

N_R = Recorder noise (RMS)

Clearly, from this point of view alone, the integrator is best positioned as far back in the system as possible. There is another distinct advantage in performing integration after differencing. The differencing process involves the subtraction of two very large numbers. Small errors in track to track matching can cause significant deviation from the ideal zero mean value of background which should be achieved. Post difference integration would reduce this deviation in the mean value of background by $1/\sqrt{n}$. Likewise, other difference errors caused by misregistrations and scintillations would also be reduced.

As stated for photocathode integration, the optimum integration is achieved when the integration time is equal to the dwell time. Figures 5 and 6 show the gain in S/N for various satellite velocities for the 1^o and 3^o FOV.

Because no one choice of integration time is optimum, the integration mode has been made selectable with a choice of 1, 4, or 8 frames.

Integration is accomplished by summing the output of fixed track recordings (fixed heads) which sequentially record frames from the output of the difference processor. Figure 6 schematically shows the

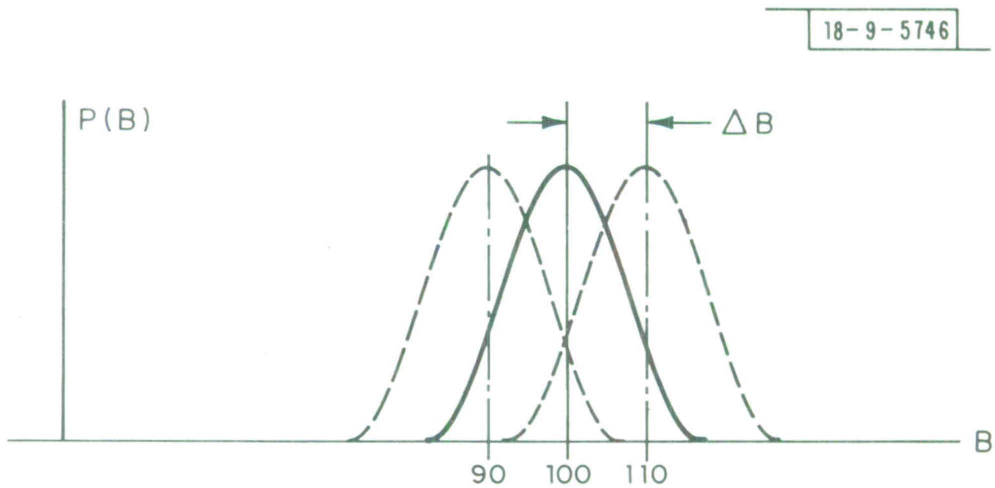

Fig. 5. Variation of signal level due to background shading.

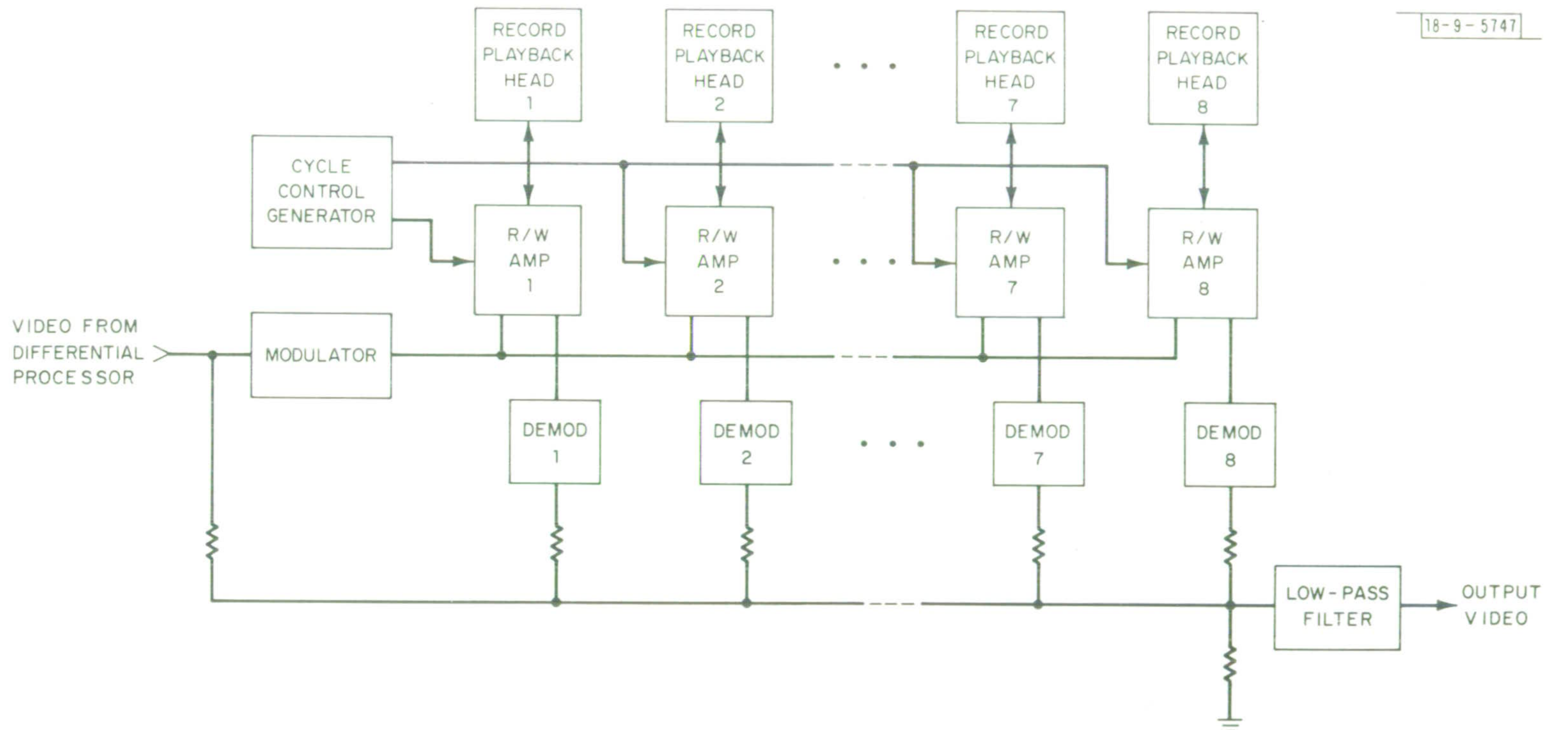

Fig. 6. Video disc integrator block diagram.

summing arrangement for the eight heads. There is always one head in the record mode which disables that output from the summing network. Figures 7 and 8 show the effect of integration gain for a low amplitude Gaussian distributed point targets.

In the configuration shown, only the sum of 1 or 8 frames are available. In order to implement the other intermediate step, some manipulation of the cycle control logic is required. For a sum of four, two tracks are recorded simultaneously in the integrator. This is not an ideal configuration because the output of the summing network is reduced to 7/8 amplitude, i.e., it is the sum of three frames twice and one frame once. However, the degradation is not serious and close enough to the ideal not to warrant the complex switching required to reconfigure the network. This technique effectively folds the integration by repeating contributions from frames in successive recordings.

Figure 9 is a complete but simplified block diagram of the Video Disc Recorder. It has been built to be used as a "stand alone" system, i.e., an operator aid or in conjunction with the signal processor to be described in the second half of this report. A more complete description of the recorder giving performance specifications and circuit details is contained in the final report.[2]

Figures 10 and 11 show the actual hardware. Figure 10 is a picture of the complete Video Disc Recorder which occupies approximately half the total rack space. The choice of the large rack was simply to make the equipment decor compatible with the rest of the GEODSS site hardware.

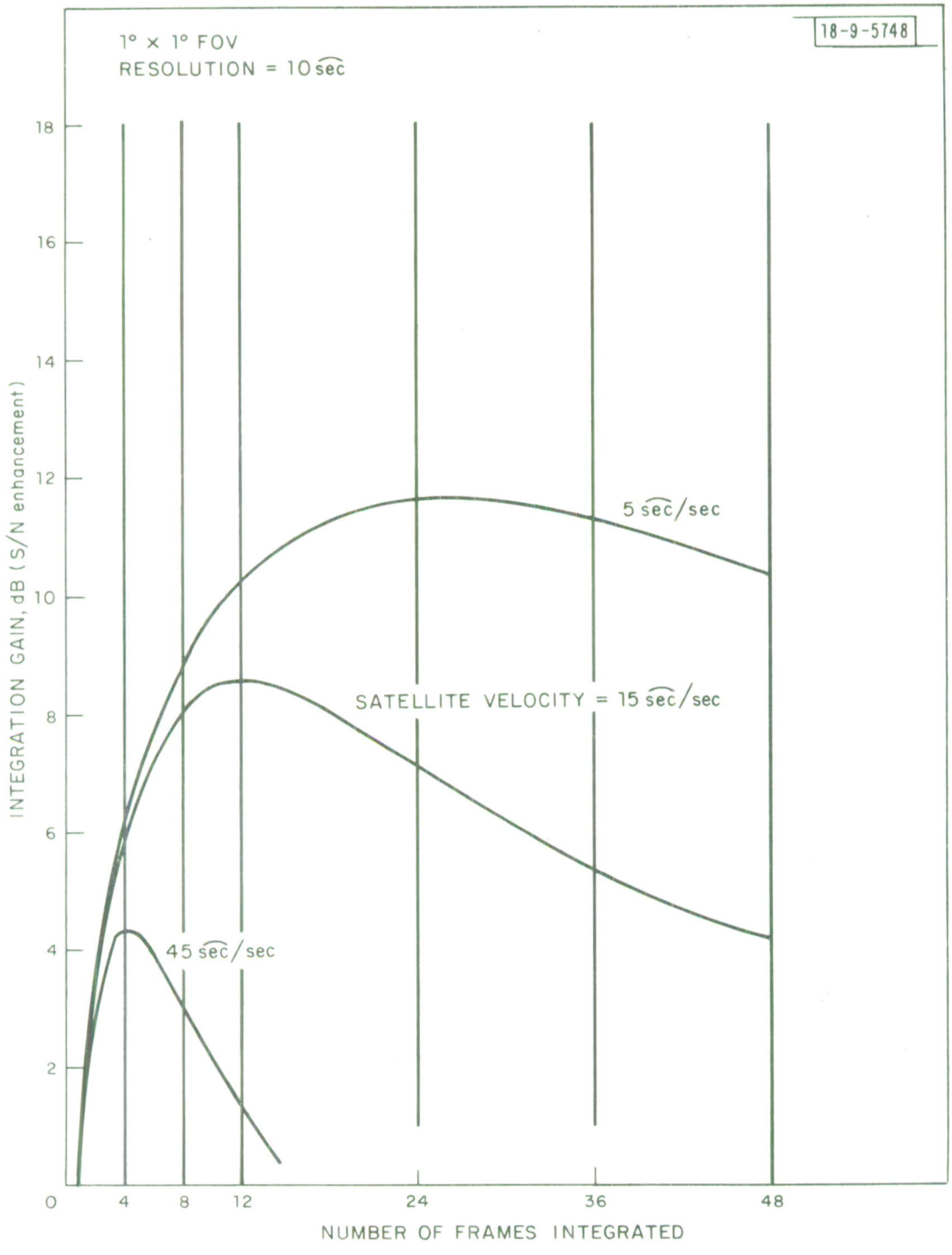

Fig. 7. Calculated integration gains (1° x 1°) FOV.

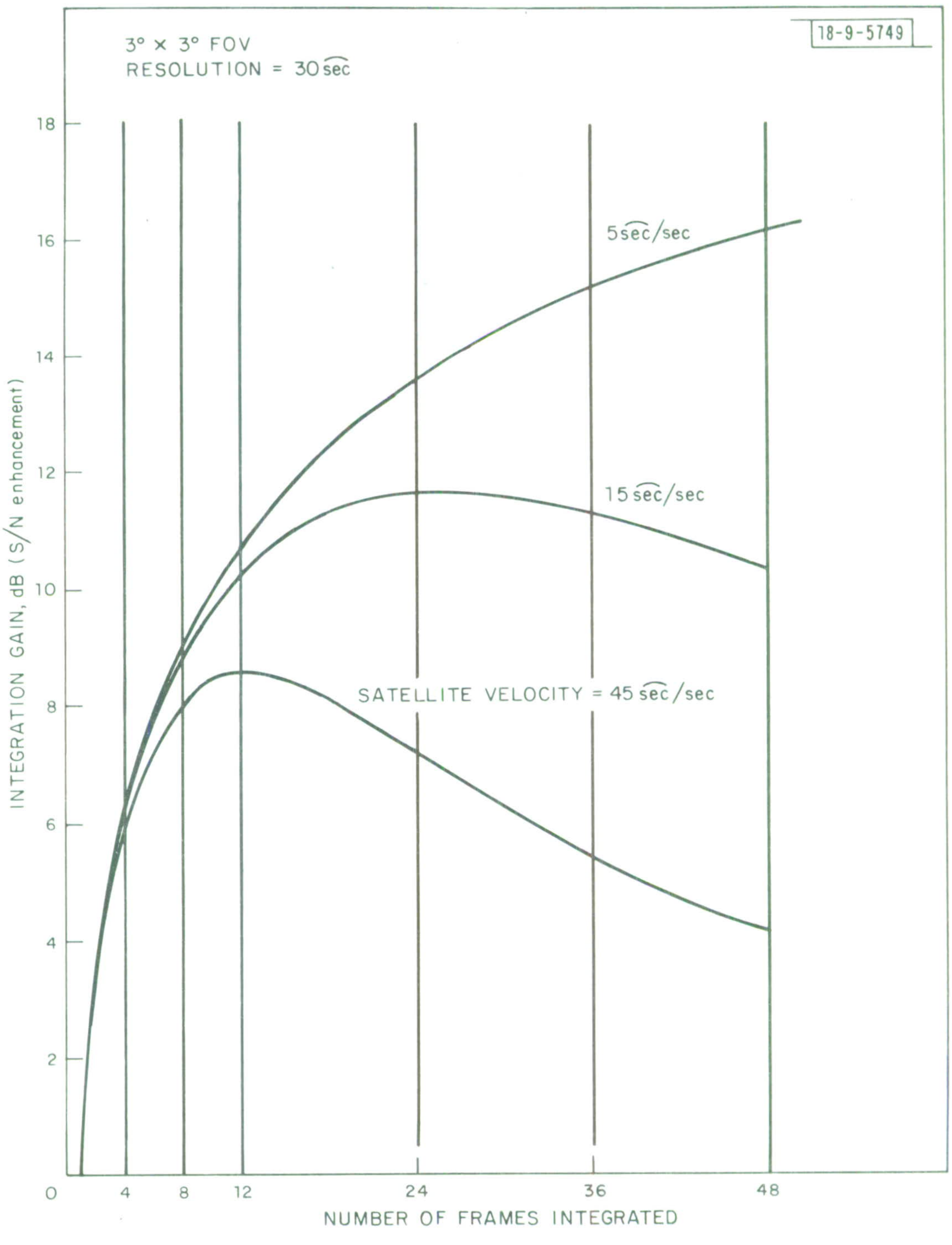

Fig. 8. Calculated integration gains (3° x 3°) FOV.

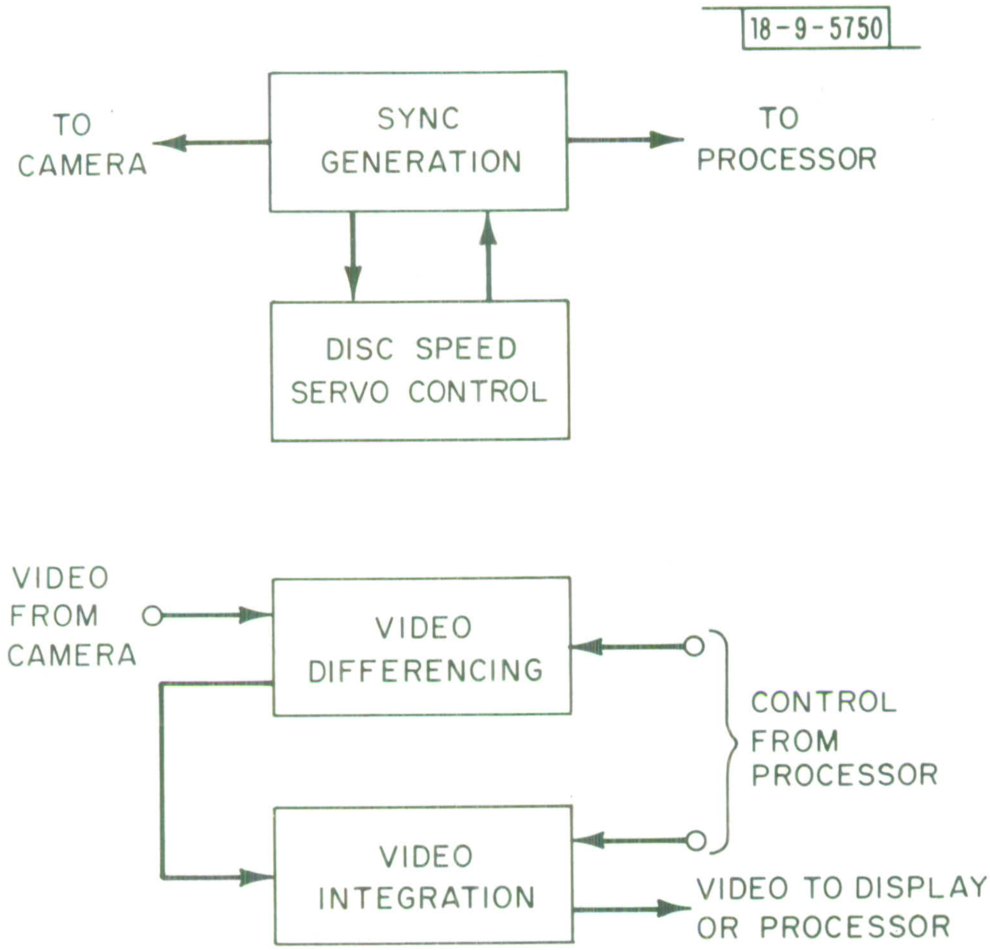

Fig. 9. Video and synch signal distribution system.

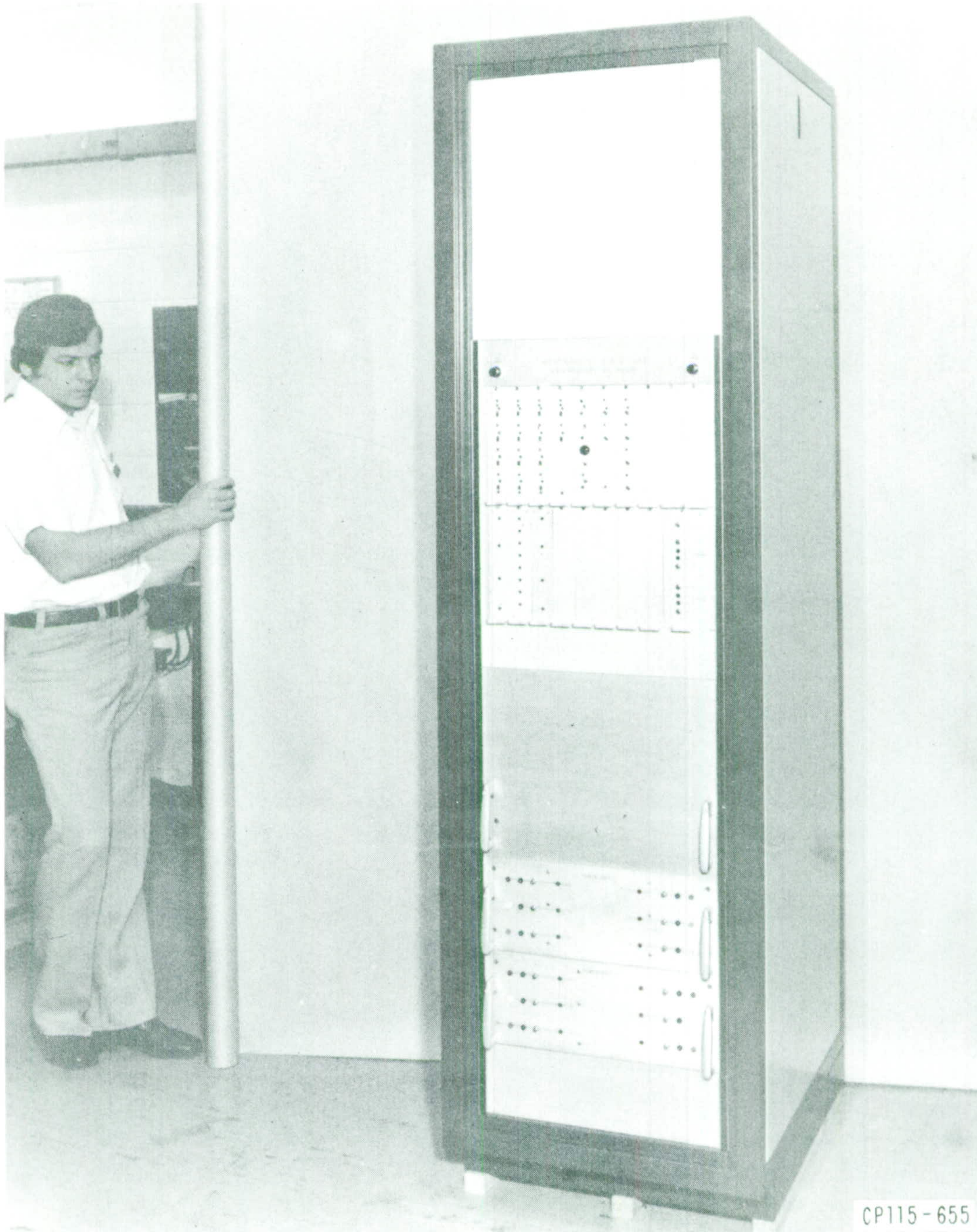

Fig. 10. Westinghouse disc processor (full rack).

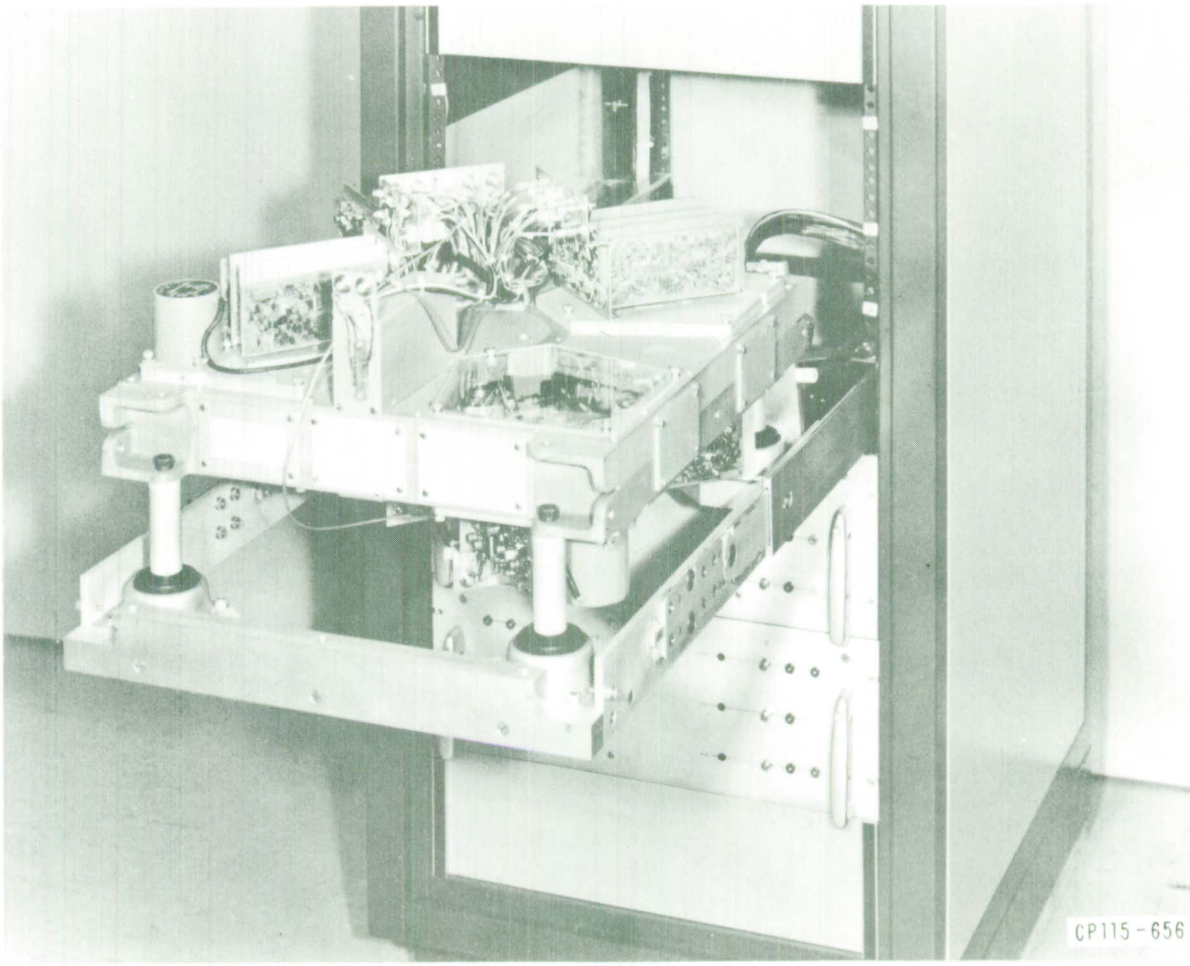

Fig. 11. Video disc (closeup).

Figure 11 is a closeup view of the rack with the disc front panel removed and the disc extended out of the rack to show the mechanical configuration of the various components.

2.0 AUTOMATIC DETECTION

After analog video differencing and integration, the video signal has been conditioned about as far as is practical for detection. Redundant information, i.e., stars, have been removed and the signal to noise ratio of the wanted signal has been enhanced as far as possible. The detection problem now is to set a threshold low enough to detect the wanted signal and yet high enough to yield an acceptable false alarm rate. The problem is shown graphically in Figure 12.

The signal is present of course in only one or two resolution cells, whereas the noise is present in all cells. If the entire FOV is marked off as a grid of 250 x 250 cells, there are 62,500 cells per picture. At a false alarm rate of 10^{-3} there would be 62.5 false alarms per picture (frame). At 30 frames per second this would be 1875 false alarms per second, which is by itself clearly unacceptable. If an arbitrary criterion such as one false alarm every ten seconds were chosen, the false alarm rate would be something less than 10^{-9} which would require a 16 to 20dB signal to noise ratio for detection. While such systems have been proposed, the performance in comparison to a human operator would be very poor indeed.

One advantage that a human operator has over an automatic detector is the ability to sense the random nature of the noise and the consistent nature of the signal. That is, the noise distribution is random across the FOV from frame to frame whereas the signal is stationary. In other words, the operator automatically decorrelates the noise and correlates

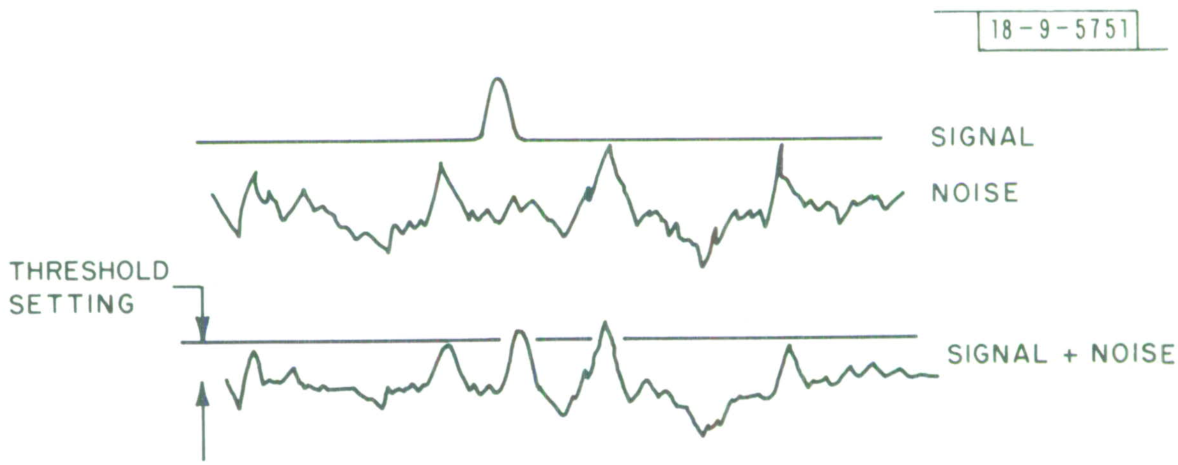

Fig. 12. Hypothetical video voltage waveforms (noise and signal + noise).

the signal. A machine which could store detection locations and then compare them on successive frames could perform a similar operation.

2.1 CFAR (CONSTANT FALSE ALARM RATE) DETECTOR

The need for a CFAR detector has been alluded to several times previously in this report. However, without going too deeply into probability theory, some justification of this technique based on statistical principals would be helpful. Figure 13 represents the probabilistic distributions of noise and signal plus noise, or more accurately the probability density functions of noise and signal plus noise.

The noise is present everywhere in the FOV and the signal presumably in one or two resolution cells. The figure shows the probability $P(\nu)$ that the noise (or signal plus noise) will have any particular voltage value (ν) on any sample. The total area under the curve is the probability that it will take on any value and of course that probability $\equiv 1$. Also shown in Figure 13 is a threshold (t). If the video voltage exceeds that threshold a detection is generated. When the noise alone exceeds that threshold it is called a false alarm. If a sufficient number of false alarms are counted (a statistically large number), that count divided by the number of samples taken will equal the integral under the tail of the curve as indicated by the crosshatched area and is called P_x, the probability of a false threshold crossing.

The signal which is some fixed value of voltage (S), when summed with the noise has a distribution similar to the noise but is displaced

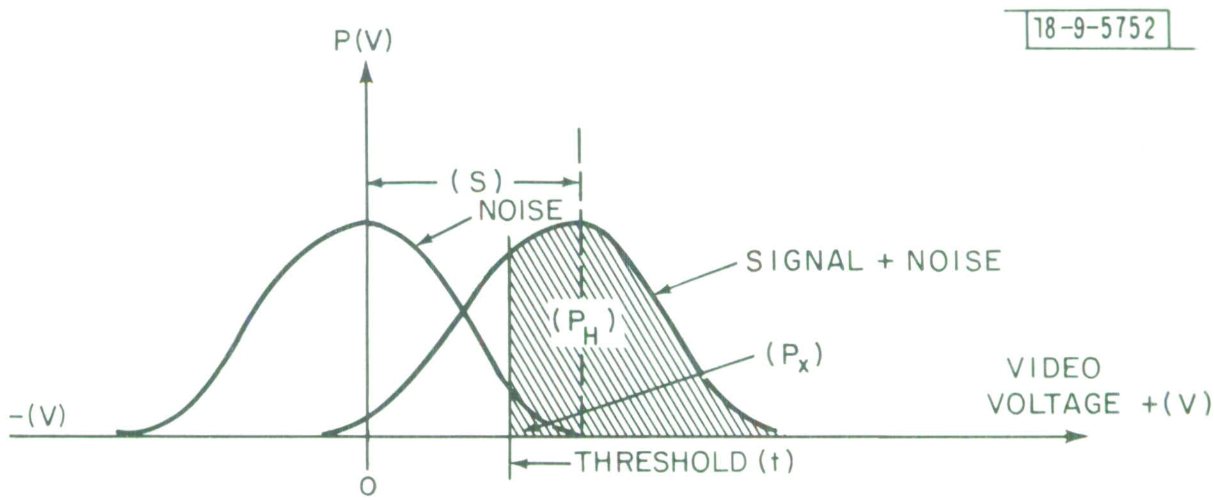

Fig. 13. Probability densities (noise and signal + noise).

from the mean by the voltage (S). Therefore, the probability of the Signal Pulse noise being greater than the threshold is higher than noise alone. The probability that the signal plus noise will be greater than the threshold is called P_H, the probability of a true threshold crossing.

If a threshold can be set on the basis of false threshold counts, i.e., if a statistically large number of false thresholds are averaged, then the operating level of the threshold is known with respect to the noise and the P_H for any given signal to noise ratio is also known. Further, if the false threshold crossing rate is set at the maximum tolerable, then the threshold is set for maximum sensitivity.

In the description of the difference process, it was pointed out that the noise (night sky background) was monopolar video, i.e., it had some mean value (M) greater than zero as shown in Figure 14.

That value (M) is a function of the magnitude of the night sky background, but is not uniform across the FOV. Such effects as shading and blemishes in the sensor, vignetting in the telescope and clusters of high intensity background will cause it to vary such that it would be difficult if not impossible to set a threshold with respect to the monopolar noise. Fortunately, the subtraction process removes the mean value of background and makes it zero everywhere regardless of any stationary effects such as shading, etc. However, the subtraction process is not perfect; some small variation due to track to track nonuniformity will cause the mean value to vary to about zero from frame to frame.

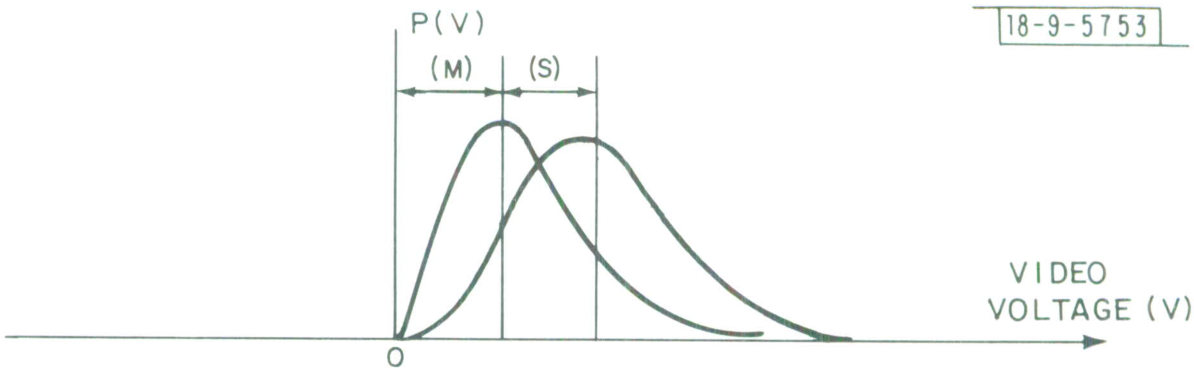

Fig. 14. Probability density of video noise background before subtraction.

Since the mean value of the background is by definition zero after subtraction, and the expected signal will occupy only a few resolution cells on a line, a simple first order matched filter will remove any slow variations in background. In simple terms, a short time constant network following subtraction removes any slow background variation due to such things as hum induced shading or atmospheric effects. This technique is commonly used in CFAR radar processes.

The implementation of the CFAR detector is rather straightforward but varies somewhat from the CFAR detectors normally used in radar receivers. The usual approach is to set a threshold at some fixed level and vary the gain of the receiver until the desired FAR is achieved. This method effectively brings the noise to the threshold. However, since this was designed to be a "stand alone" system it has been implemented by bringing the threshold to the noise. Because there is an AGC system in the recorder, the system is actually a hybrid. Figure 15 shows the basic CFAR detector.

The signal from the camera is fed to the input of the comparators where it is compared to a threshold voltage (t). If the signal voltage is greater than the threshold, an output is generated. The lower comparator has the same threshold attenuated by [A] such that it provides roughly ten times the amount of threshold crossings. The reason for this is to provide a good statistical average of threshold crossings and to prevent the system from being biased by bright star residues which will be handled separately.

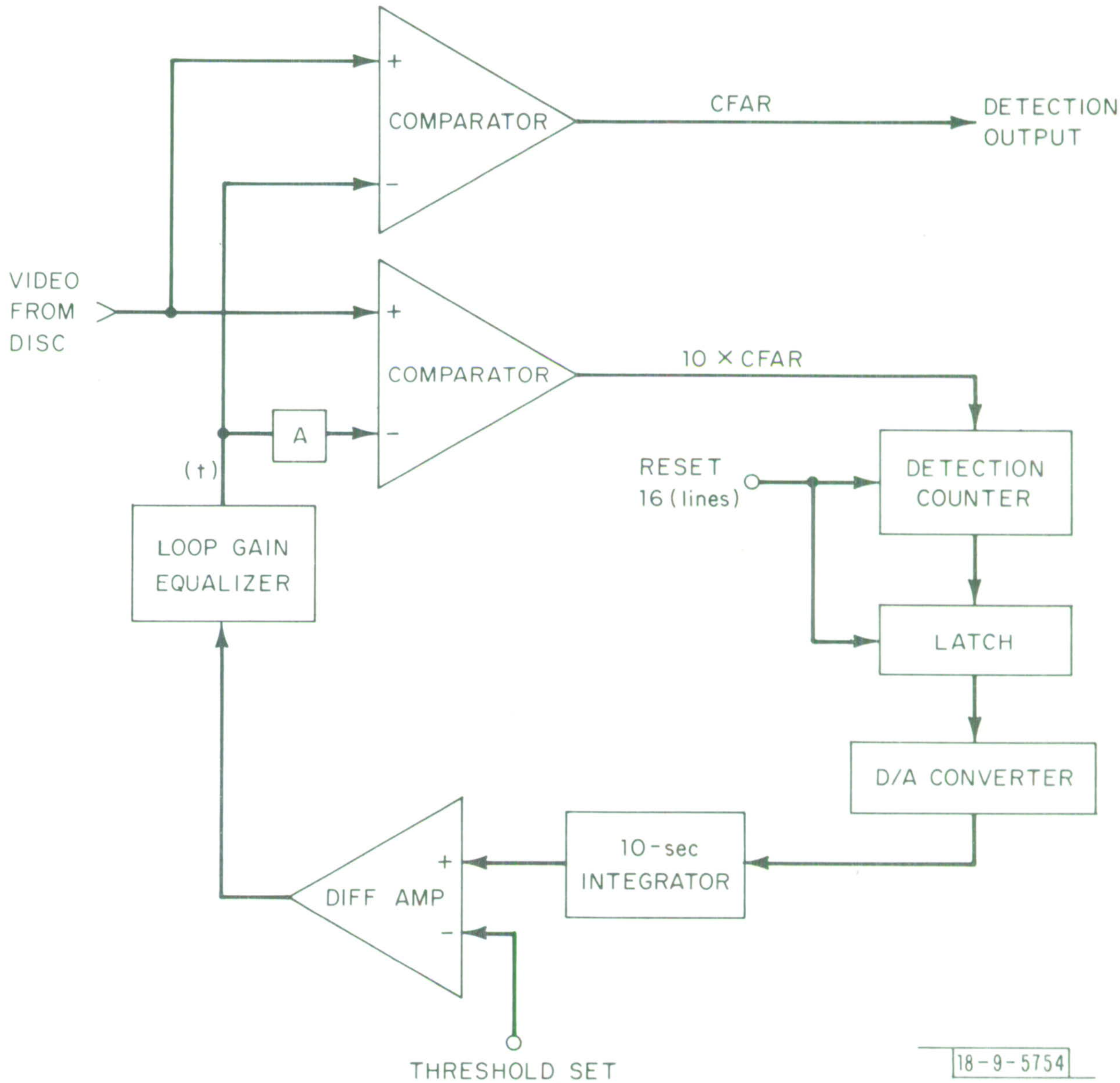

Fig. 15. CFAR detector.

The output of the 10 x CFAR comparator is fed to the detection counter which is reset every 16 lines. The latch is used to store the count from the previous 16 lines and its output is fed to a digital to analog converter whose output is smoothed by the ten second time constant integrator. The differential amplifier compares this voltage with a preset CFAR threshold value and provides a nominal loop gain of 100. The overall loop time constant then is 0.1 second and the overall loop tracking error is on the order of ± 0.5kHz over a 40dB dynamic range with a nominal CFAR rate of 6.128kHz.

The loop gain equalizer is necessary to stabilize the system over a wide dynamic range. The loop gain is determined by $\Delta(t)/\Delta F$, i.e., the change in threshold voltage for a given change in frequency. At high noise levels a relatively large change in threshold voltage is required to effect a given change in frequency. On the other hand, at low noise levels, a very small change in threshold voltage will cause a large change in frequency. The loop gain equalizer compensates for this by reducing the gain as the threshold is decreased for lower noise levels. A more complete description of this circuit is given in the Appendix.

2.2 DETECTION RESOLUTION

After the detection, the remainder of the processing is now digital, i.e., ones and zeros. A one corresponds to a threshold crossing and a zero to no crossing. In order to operate a digital correlator it is necessary to assign these ones and zeros to discrete matrix locations which correspond to the original X-Y location in the FOV. The number of

resolution cells in the detection matrix should not exceed the number of resolutions cells in the sensor. The sensor is the limiting factor in the precision of measurement. Increasing the detection matrix resolution further than this only increases the data processing load. In fact, there is some advantage in decreasing the detection resolution as will be described in the discussion of the correlator.

Whatever method is chosen to generate the matrix, it must be "hard locked" to the camera sync to assure that each matrix location appears in the same X-Y location on each succeeding TV frame. The TV raster is made up of two interlaced fields of 262.5 lines each. Of this, 20 lines are blanked on each field. Therefore, an eight bit word would describe the Y location in a given field. The alternate field contains practically no information that was not in the first field because of the limited resolution of the sensor. The most logical thing to do analytically would be to sum the alternate fields line for line before detection, but this becomes rather complex in terms of hardware. The next best choice is to carry the alternate field through the processor with the addition of one bit for field information. Carrying the alternate field effectively reduces the memory capacity of the correlator by a factor of two. However, this is not a serious penalty and the redundancy slightly improves the probability of detection which tends to offset the loss.

The horizontal resolution should be on the same scale as the vertical. Fortunately, the master clock which generates all the sync and timing for the system is at a frequency of 2.0475MHz. Exactly 234 half cycles

of this clock correspond to the interval between two horizontal blanking pulses. Again, this requires an eight bit word to describe the X-locations. The matrix is now described in a 16 bit word corresponding to 242 elements vertical by 234 elements horizontal.

2.3 BRIGHT STAR BLANKING

Because the subtraction process is imperfect, some residue from the edges of bright stars will remain after subtraction. These residues if allowed to pass would correlate and therefore must be somehow erased. The simplest and most straightforward way to do this is to find the bright stars in the original unsubtracted picture. And, if a detection occurs within the vicinity of a bright star, reject it. This results in some penalty in detection probability, but not much. Obviously, if a satellite were over a bright star, it could not be detected in any case. The method used is shown in Figures 16, (a) (b) (c) and (d).

Figure 16(a) shows a small area bright star on the order of one resolution cell in diameter that happens to overlap four detection cell locations, the corresponding blanked area is 12 cells. Figure 16(b) shows the same star centered in a single detection cell and the blanked area is nine cells. Figure 16(c) shows two small area stars adjacent and the blanked area is 17 cells. Figure 16(d) shows locations and the blanked area occupies 25 cells.

The difficulty now is to analytically predict from these simple models how much area is lost due to blanking with an ensemble of real

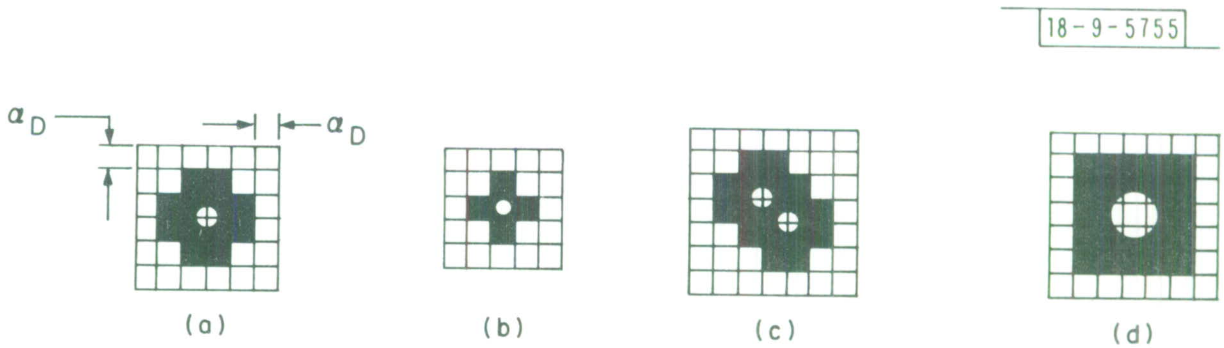

Fig. 16. Bright star blanking area.

stars. However, if we were to take a rough estimate of 12 cells per star, this would probably be fairly accurate for moderate star densities. As the star densities increased, the lost area per star would tend to decrease as more and more blanked areas overlapped. Using these criteria we would have a total lost area of approximately 20 percent for a star population of 1000 stars.

Figure 17 shows schematically how bright star blanking is accomplished. Bright stars are detected at 80 percent of the peak white amplitude in the bright star detector. Because the video from the camera has not been processed as much as that from the disc, it always leads that video by one to two microseconds and delay equalization must be provided to assure proper registration. This is accomplished after detection by selecting outputs from a shift register. Three taps are selected and summed in the final shift register to provide the full leading to trailing blanking interval along the line. A one line delay is provided to generate the previous line blanking. This is summed with the on line blanking and used to inhibit the CFAR detections. The blanked detection train is then delayed one line and blanked again to provide the trailing line blanking. A more complete description of this circuit is given in the Appendix.

In the previous section on the video disc, the minimum delay before subtraction was set up on the basis of (α/ω). Now that α_D (the detection resolution) and bright star blanking have been introduced, these must be taken into account to assure that the satellite is not blanked by its

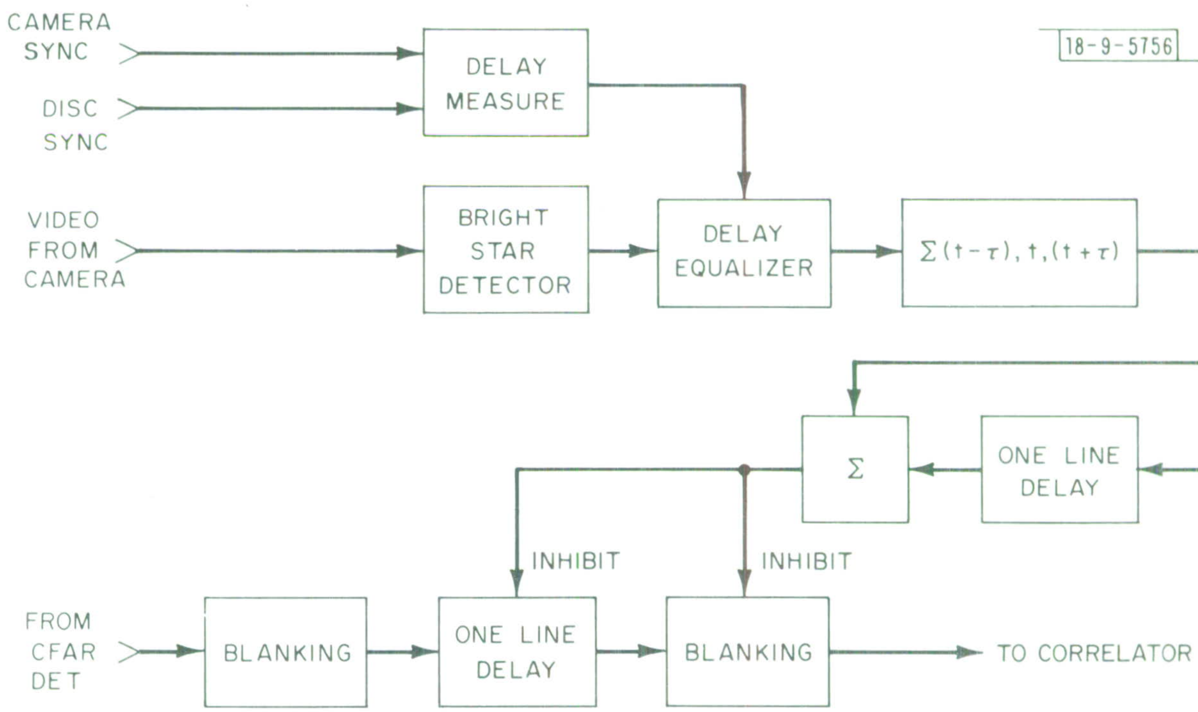

Fig. 17. Bright star blanking circuit.

own detection if it should happen to be very bright. Figure 18 is a new plot of ω vs. T, taking these factors into account.

2.4 CORRELATOR

One possible correlator configuration that could be implemented to sort out the false alarms is shown in Figure 19.

Detection locations are written into memories one and two on alternate frames. While one memory is writing, the other is reading. The one being read is one frame behind the input from the detector and is compared to it. If there is a detection location present in both the memory "AND" the input, the detection is correlated and sent to the alarm circuit.

Such a correlation scheme will reduce the false alarm rate by the square of the input false alarm rate, i.e., if the input false alarm rate were 10^{-3}, the output false alarm rate would be 10^{-6}. Likewise, additional correlations, e.g., 3 out of 3 would reduce it by the cube and so on. Unfortunately while such a scheme recognizes the randomness of noise, it does not recognize the consistent nature of the signal. The probability of detection decreases by the same power as the probability of false alarm. For example, an input probability of detection of 0.7 would be reduced to 0.5 at the output.

Another class of correlator which does recognize consistency while rejecting randomness is the majority logic correlator. The criterion for accepting a detection is the same as that used for sporting events, i.e., 2 out of 3; 3 out of 5; 4 out of 7; and so forth. While the false

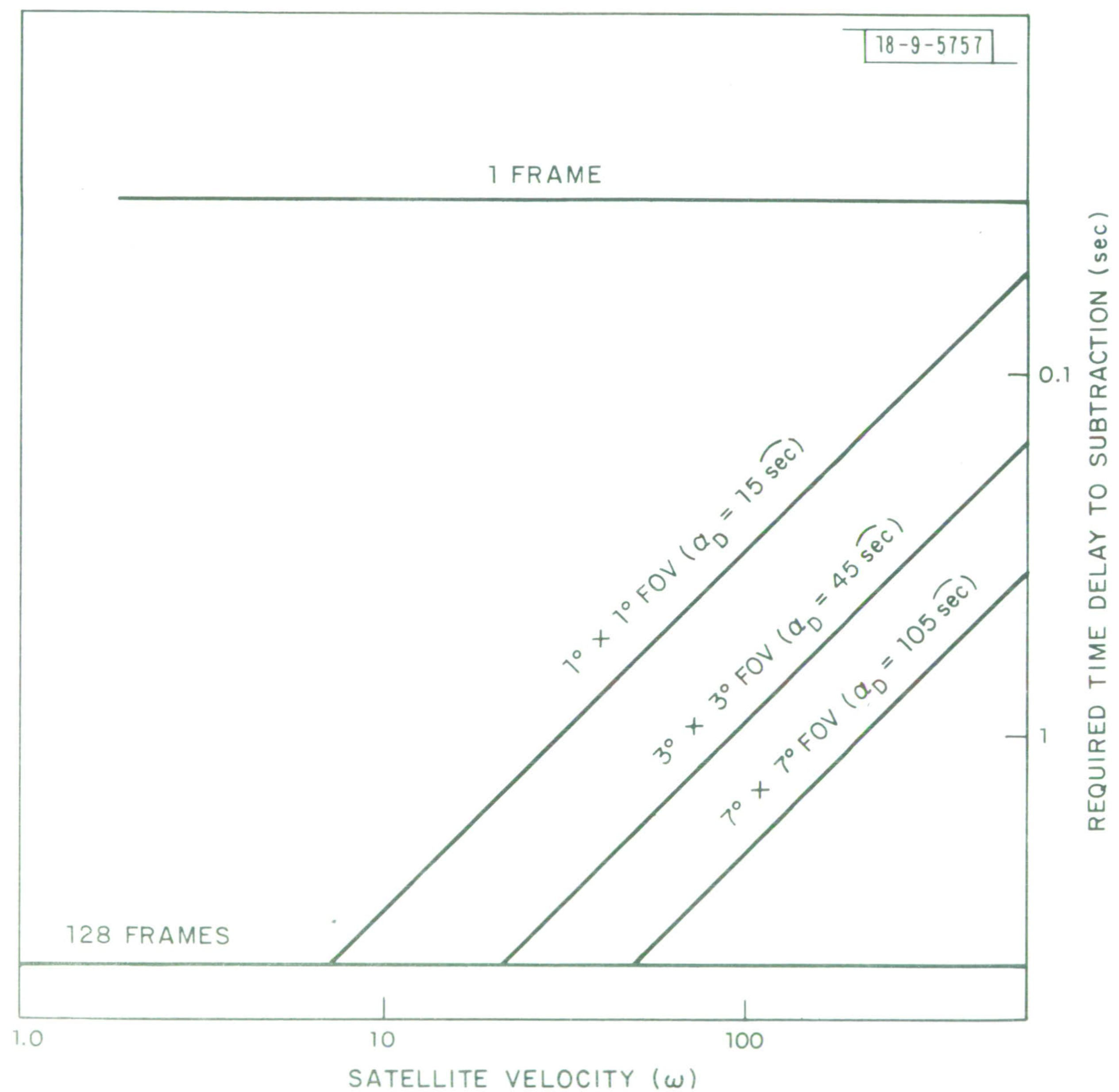

Fig. 18. Angular velocity (ω) vs required difference delay (time) with bright star blanking.

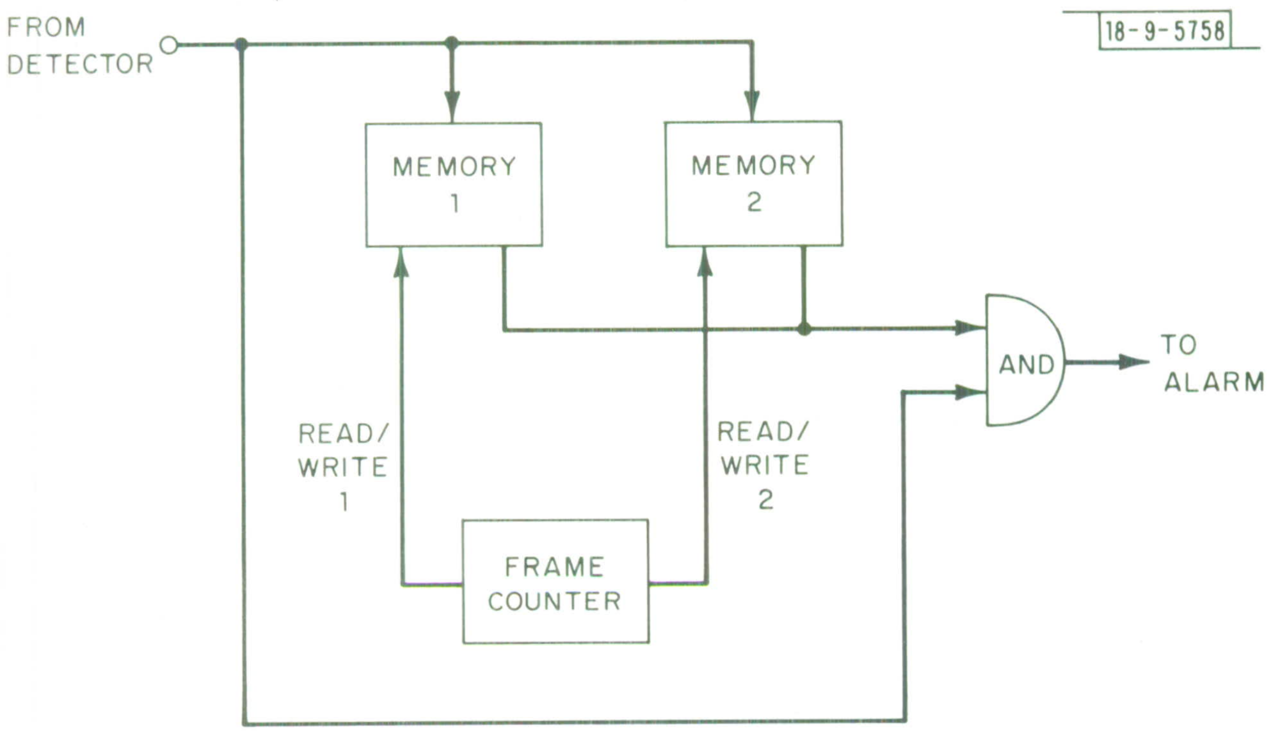

Fig. 19. Simple 2 of 2 correlator.

alarm rate does not drop quite as rapidly for this class, the P_D (probability of detection) increases for any $P_H > 0.5$. Table I lists the formulas for calculating the P_D and P_f (probability of false alarm) for any input P_H and P_X. Figure 20 shows the output P_D for the various correlators discussed.

The correlator memories could have been implemented in any number of ways. The most logical choice would have been to add a number of digital tracks to the video disc. In this way, detection locations are automatically positioned in a time reference, and any future system would use this technique. However, in order to speed up the development program, it was decided to use solid state scratch pad memories. In this way, development of the automatic detection system could proceed and be ready for interface with the disc when it was delivered.

Figure 21 is a simplified schematic of the memory used. There are a total of eight such memories, each will store 256 detections per frame corresponding to an FAR (false alarm rate) of 1.8×10^{-3}. While one memory is writing, the other seven are reading. If desired, a lower order correlation than 4 of 7 may be selected, such as 3 of 5 or 2 of 3.

At the beginning of each frame the address counter is reset to memory location one. During the write cycle detections enable the memory, and the 16 bit number from the reset counter which corresponds to an X-Y location in the FOV is written into the memory. After each word is written, the address counter is advanced to the next memory location. In this way, detection locations are sequentially stored in

TABLE I

Process	P_f	P_D
2 of 3	$3 P_\chi^2$	$3P_H^2 - 2P_H^3$
3 of 5	$10P_\chi^3$	$10P_H^3 - 15P_H^4 + 6P_H^5$
4 of 7	$35P_\chi^4$	$35P_H^4 - 84P_H^5 + 70P_H^6 - 20P_H^7$
3 of 3	P_χ^3	P_H^3
4 of 5	$5P_\chi^4$	$5P_H^4 - 4P_H^5$

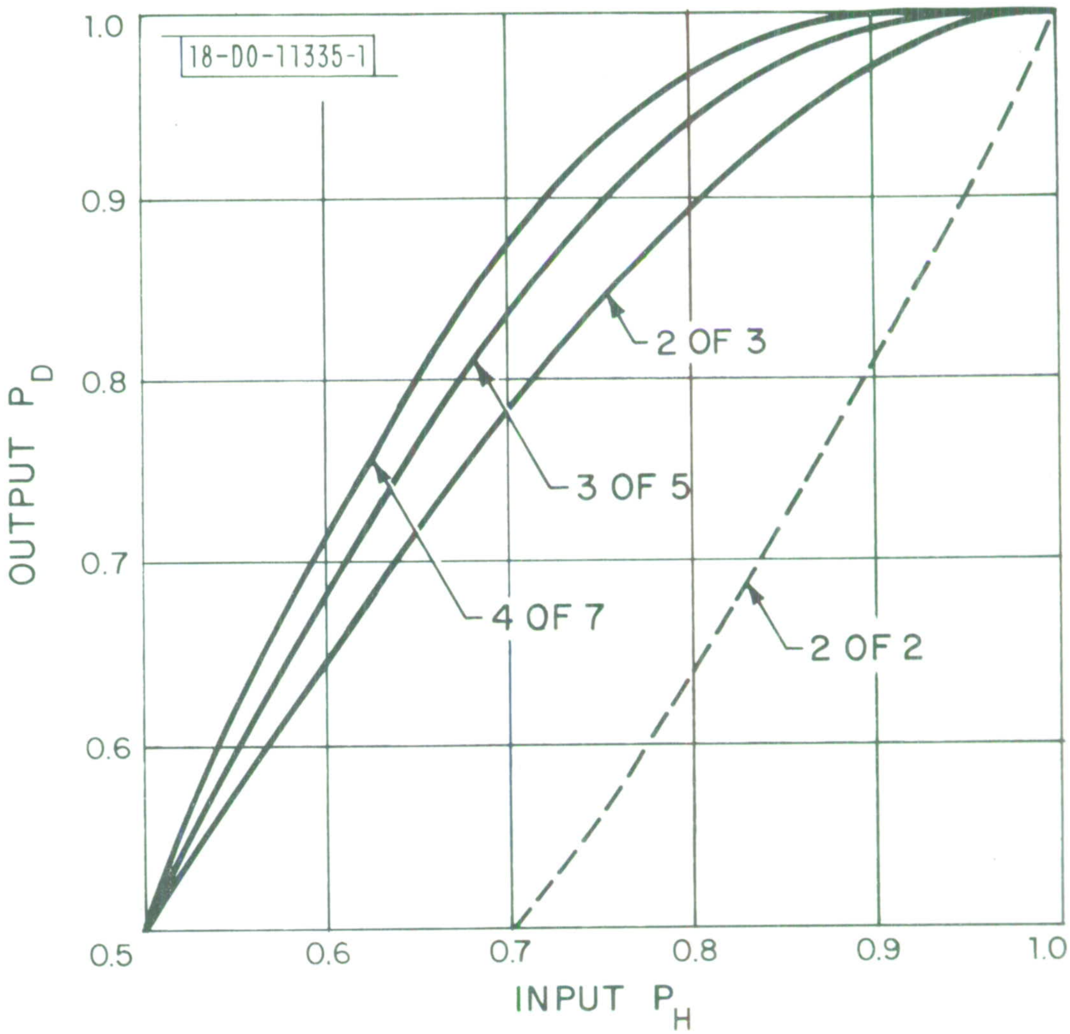

Fig. 20. Majority logic correlator detection enhancement.

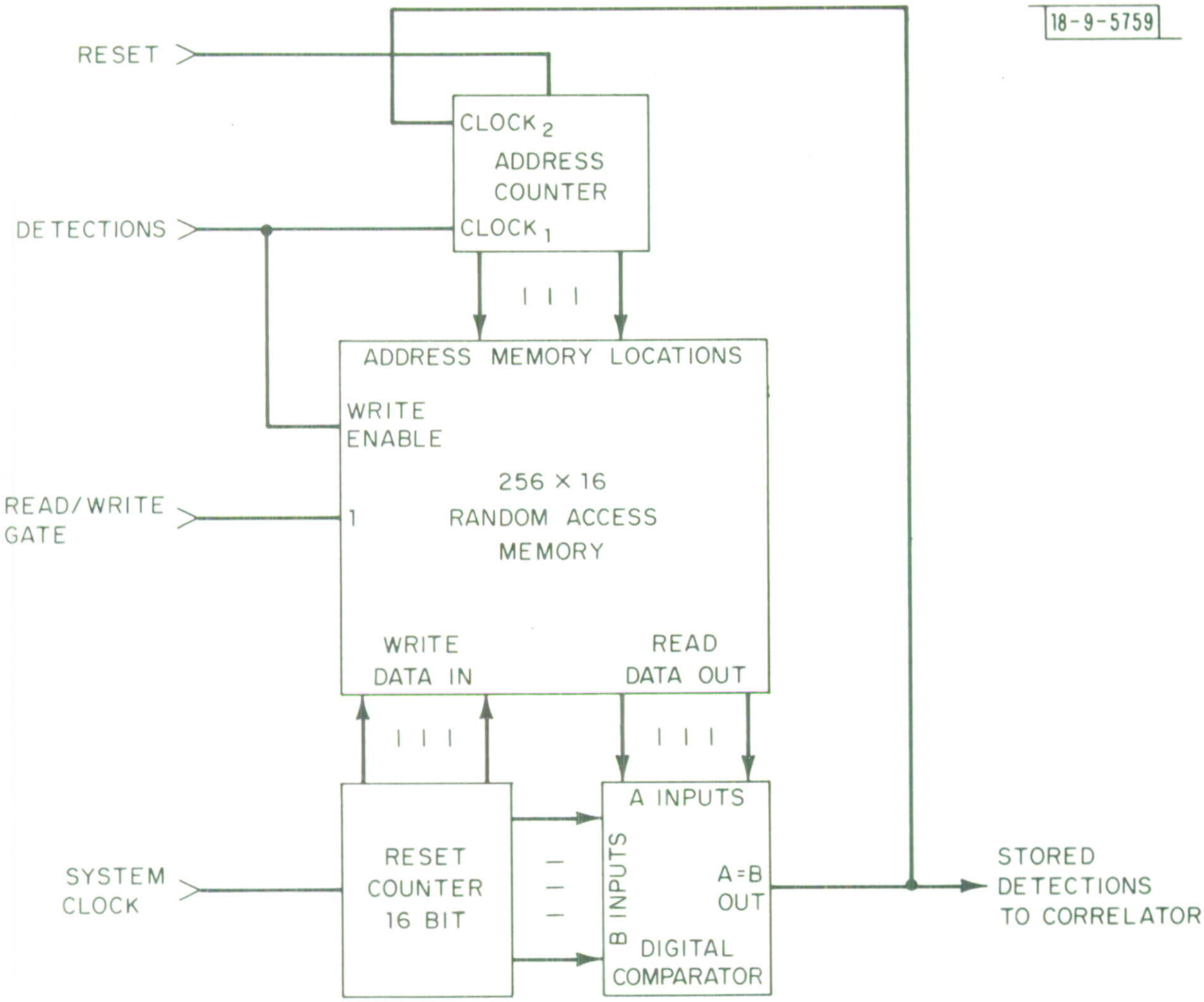

Fig. 21. Correlator memory.

the random access memory. During the read cycle, the address counter is again reset to memory location one. The output of the memory is now compared to the resel counter and when they are coincident, a pulse is generated and sent to the correlator, and the address counter advanced to the next memory location. A more complete description of this circuit is contained in the Appendix.

The correlator itself, i.e., the circuitry that decides if 2, 3, or 4 detections are present is a simple "Read Only Memory." This memory has been programmed from a truth table corresponding to all the possible combinations of detections. Outputs corresponding to 2, 3, 4, or 5 detections are available and operator selectable depending on the correlation mode chosen and the function. More detail on the functional use of the correlator will be given in the description of the Cursor Generator and Bell Ringer descriptions.

The choice of correlation mode chosen depends on two factors, the velocity of the satellite (ω) and the processing time required. The first is fairly obvious; for very high velocity satellites, the dwell time in a resolution cell is very short and a large number of correlations is not possible. Figure 18 which shows the minimum time delay required before subtraction is possible also shows the maximum correlation time available. However, this is before integration. If a number of frames are integrated, the statistics of the noise are not decorrelated since each succeeding frame will contain contributions from the previous (n - 1) frames if (n) is the order of integration.

Because of this, it is necessary to wait (n) frames before taking the next sample frame for correlation. Combining this information with the dwell time gives the maximum number of frames that may be correlated as:

$$M = \frac{\alpha_D}{(2\omega)} \times \frac{30\ \text{FRAMES}}{\text{SEC}}$$

which simply states that the satellite may not be displaced more than 1/2 resolution cell over the correlation interval. Note that α_D corresponds to the detection resolution ($\alpha_D \approx 1.5\alpha$) and not the sensor resolution. Figure 22 shows the limit of correlation for various integration intervals and the FOV's versus (ω). This chart would be used to set up the correlation mode and integration interval in a tip-off search. For example, assume the system is operating with the 31" telescope, i.e., the $1^\circ \times 1^\circ$ FOV and the satellite being searched for is at synchronous (15 $\widehat{\text{sec}}$/sec). A choice of a 2 of 3 correlation is possible with an integration interval of four frames.

The processing time (P) required is the product of the integration interval (n) and the number of frames correlated (M), plus the minimum delay to subtraction:

$$P = nM \times \frac{\text{SEC}}{30} + T_{D_{MIN}}$$

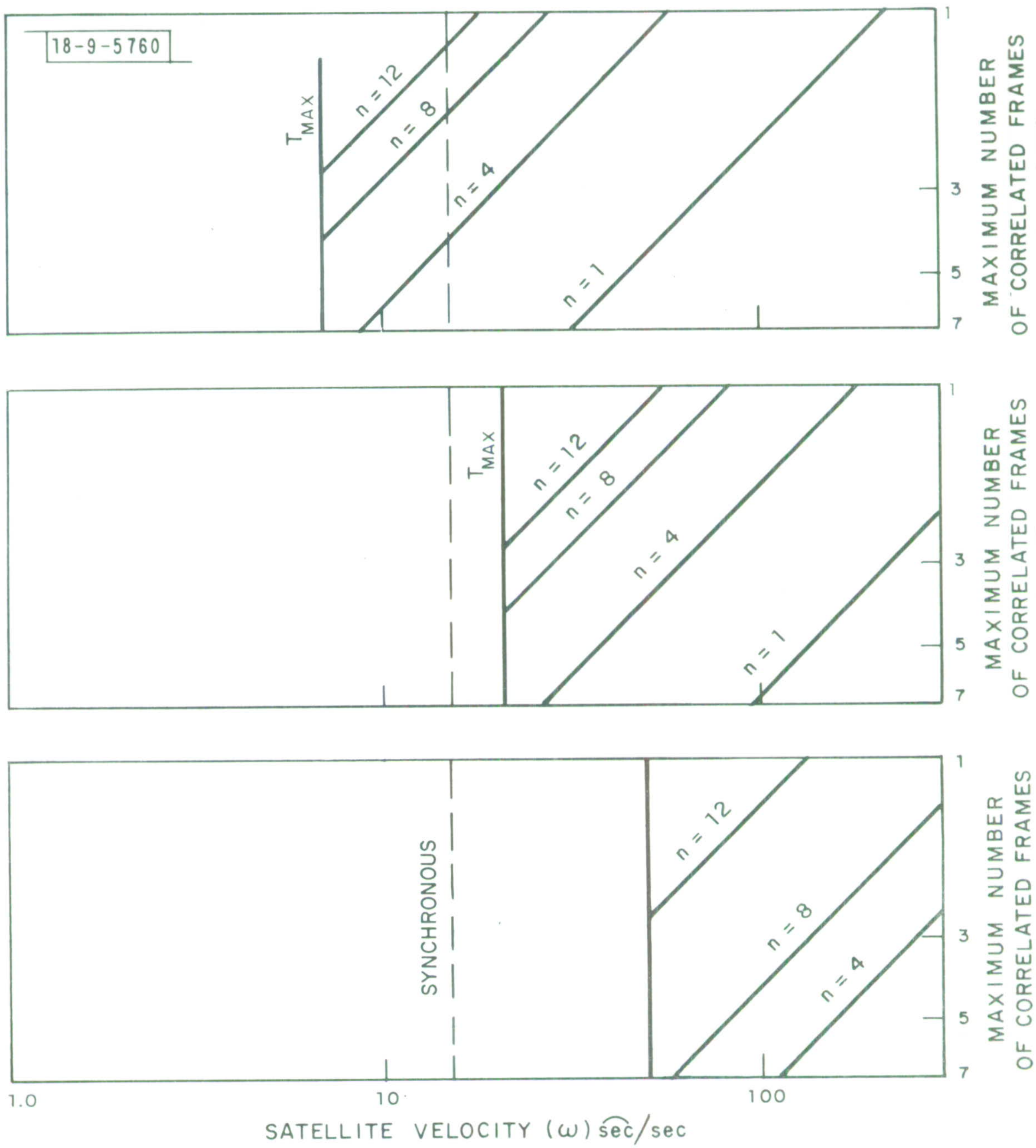

Fig. 22. Satellite velocity (ω) vs maximum correlation interval.

Clearly, $T_{P_{MIN}}$, is strictly a function of $(\alpha_D/2\omega)$ which is directly related to the FOV. Depending on the night sky conditions and the brightness of the satellite it may be of some advantage to go to the wider FOV on the 14" telescope in some cases. The integration interval chosen is bounded by the limits shown in Figure 22. Any correlation below the lines (3, 5, or 7) is possible, anything above is not. However, if a satellite is bright, it will occupy more than one resolution cell.

It shold be noted that it is not possible to optimize integration gain and correlation interval simultaneously. In order to do this, it would be necessary to reduce the detection resolution α_D. In effect this would be trading off positional information (X-Y precision) for signal to noise. While this may seem like a worthwhile thing to do, the maximum gain over the present system configuration is about 2dB and the penalty in complexity of hardware is considerable.

2.5 ALARM AND CURSOR GENERATORS

The ultimate purpose of all the signal processing previously described is to generate a signal which would:

1. Remove all clutter (stars and background) from the display and show only the satellite in the FOV.
2. Generate a cursor (box) which when added to the video surrounds the satellite detection, thus providing an additional operator aid.
3. Sound an alarm to alert an operator than a detection had taken place and there was a satellite within the FOV.

2.5.1 FALSE ALARM RATES

The false alarm rate is directly related to the probability of detection, i.e., the higher the false alarm rate, the higher the probability of detection. However, this probability of detection increases only up to the point where the system "cries wolf" too often and then diminishes rapidly. Different alarms have a different level of tolerance. For example, a few extra cursors which randomly flick about the television monitor are not very distracting to an operator who will focus only on the stationary cursor even though it may be flickering on and off. On the other hand, a lamp that lights or a bell that rings with a frequency of once a second will be totally ignored. Likewise, a computer receiving false alarms at the rate of 30 words per second is not especially burdened by the computational load in sorting out these false alarms.

Therefore, in order to maximize the probability of detection and minimize the "wolf crying," two separate correlation modes have been chosen for the "bell ringer" and the cursor generation or computer detection word. Table II lists the companion correlation modes and their respective false alarm rates. Figure 23 shows the corresponding input/output P_D for the Bell Ringer correlations.

Clearly, for every case except the 3 of 3 for the "Bell Ringer" the false alarm rates are acceptable. One false alarm every 1.2 minutes is definitely "wolf crying." Therefore, one additional step has been taken to make the alarm virtually foolproof. The "Bell Ringer" has been designed as a two step alarm. On the first detection a two second gate

TABLE II

FRAMES INTEGRATED	CORRELATION MODE		FALSE ALARM RATES	
	CURSOR	BELL RINGER	CURSOR	BELL RINGER
1	2 of 3	3 of 3	33/SEC	1.2/MIN
1	3 of 5	4 of 5	12/MIN	1/1.6HR
1	4 of 7	4 of 7	4.5/HR	4.5/HR
4	2 of 3	3 of 3	8.3/SEC	18/HR
4	3 of 5	4 of 5	3/MIN	1/6.2HR
4	4 of 7	4 of 7	1.1/HR	1.1/HR
8	2 of 3	3 of 3	4.1/SEC	9/HR
8	3 of 5	4 of 5	1.5/MIN	1/12.4HR
8	4 of 7	4 of 7	1/1.8HR	1/1.8HR
12	2 of 3	3 of 3	2.8/SEC	6/HR
12	3 of 5	4 of 5	1/MIN	1/18.6HR
12	4 of 7	4 of 7	1/2.7HR	1/2.7HR
24	2 of 3	3 of 3	1.4/SEC	3/HR
24	3 of 5	4 of 5	1/2MIN	1/37HR
24	4 of 7	4 of 7	1/5.3HR	1/5.3HR

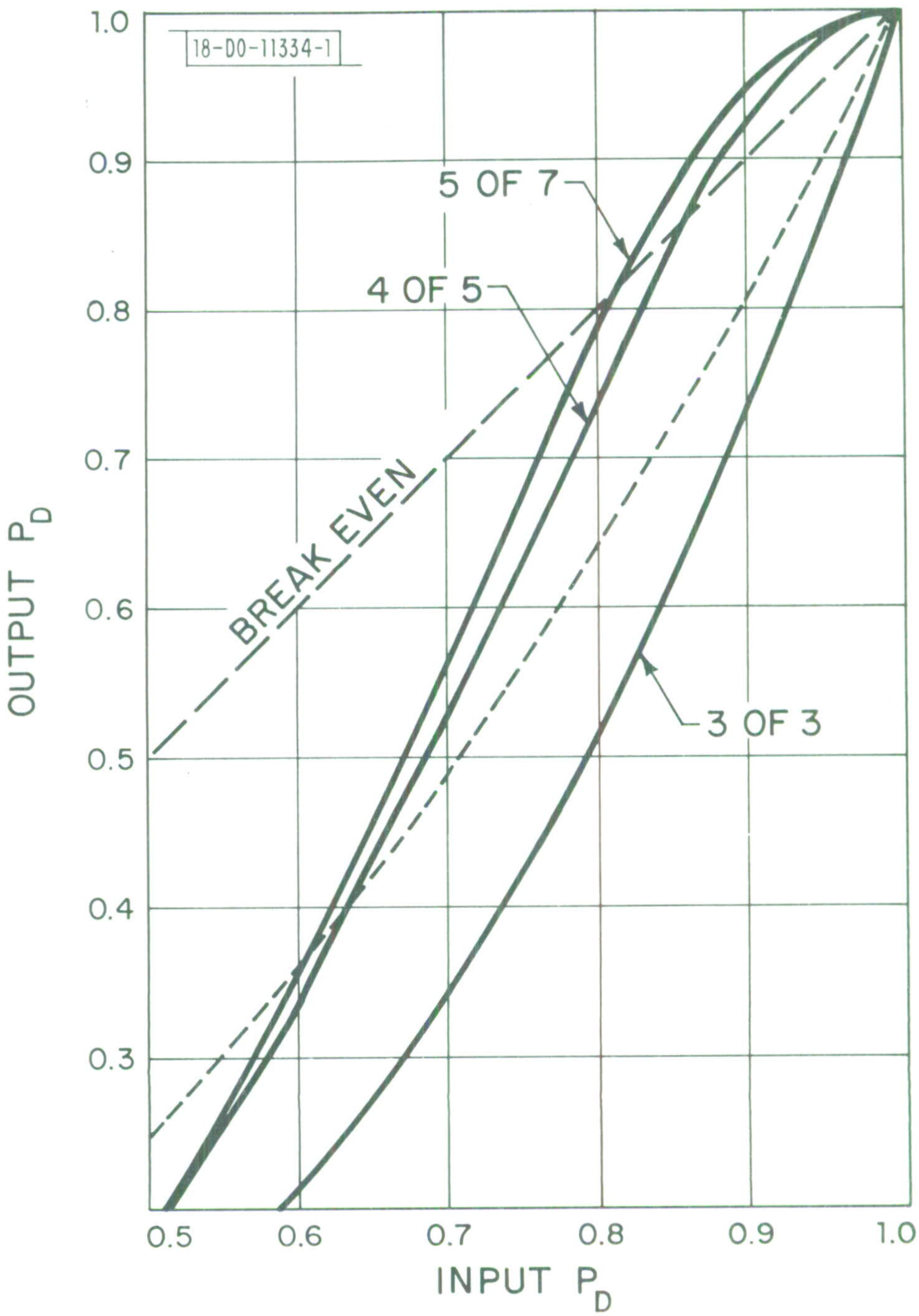

Fig. 23. Bell ringer detection probability.

is generated. If during that two seconds a second detection takes place, a red flashing "ALARM" lamp goes on and audible alarm is sounded. A complete description of this circuit is given in the Appendix.

2.6 CURSOR GENERATION

The primary purpose of the cursor is to locate a satellite within the field of view. It also acts as an alarm system which only requires a moderate amount of attention by an operator watching a television monitor. The cursor appears on the monitor as the perimeter of a rectangular box, 16 lines by 16 elements. The cursor is displayed on a monitor containing either camera video or "disc" (subtracted) video. Figure 24 is a picture taken from the TV monitors showing the cursor in both cases.

Because of the relatively high false alarm rate in the correlator output for cursor generation, and the distinct possibility of more than one satellite in the field of view, it is necessary to provide for the generation of more than one cursor simultaneously, i.e., within the same TV frame. Therefore, a maximum of four cursors may be generated within any 16 line interval and a total of eight cursors per field or 16 per frame.

Because the cursor is a box that surrounds the satellite, the cursor generation must start eight lines and eight elements in advance of the actual detection. In order to do this, detection locations are stored in a buffer memory and then read out by comparing the data in the memory to an advanced resel counter on the succeeding frame. Except for

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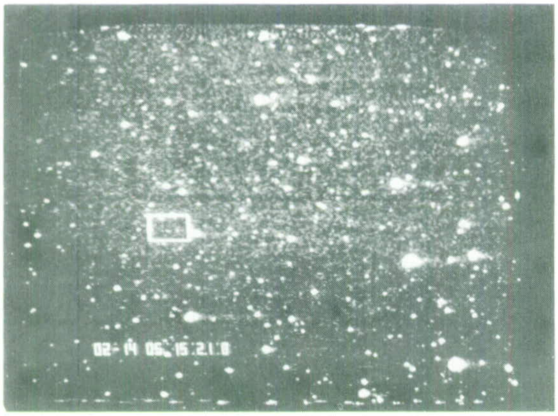
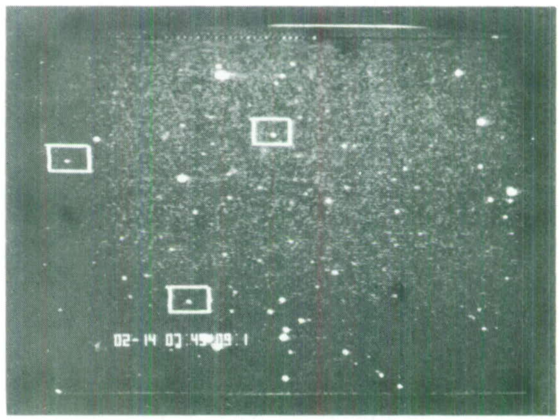
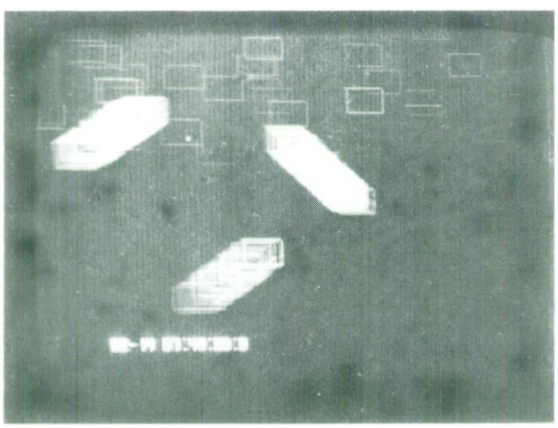


SYNCHRONOUS SATELLITE
83502 NATO I
$\approx 15^{m}.5$

THREE SMALL OBJECTS
$\omega \approx 7\ \widehat{\mathrm{sec}}\ \mathrm{sec}^{-1}$
5713 RB 19 MOLNIYA 1
7641 12 MOLNIYA 2
7540 1 MOLNIYA 3





≈1 MIN INTEGRATION
ON VIDEO REPLAY

VIDEO DISC AMTI AT
EXPERIMENTAL TEST SYSTEM
31" CASSEGRAIN WESTINGHOUSE
I-EBSICON
1.2° FOV (diag)

Fig. 24. Typical monitor displays of satellite detections.

the advanced readout, the technique used is similar to that in the correlator memory readout.

The cursor is generated by starting a 16 x 234 element counter which counts resels for 16 lines and stops. The output of the counter drives a ROM (read only memory) which generates "ones" at the appropriate places to form a box. The ROM also generates an area gate, i.e., a gate which is "one" within the entire area of the 16 x 16 element box. Because there is a delay between camera and disc video, the cursor and gate are generated with respect to the camera video and a delay cursor is generated by means of a shift register delay as for the Bright Star Blanking circuit. A complete description of the Cursor Generator is given in the Appendix.

2.7 DISC/PROCESSOR INTERFACE

Because the disc and the processor are functionally interrelated, the processor cycling logic must take into consideration the integration mode of the disc. For example, if there are (n) frames of integration, the correlator must sample every n^{th} frame. For this reason, when the control cable from the processor is connected to the disc, the disc cycling control logic is slaved to the master control panel of the processor. When the control cable is disconnected, the disc operates as a "stand alone" unit which could be used as a manual MTI system.

The control signal from the processor is in the form of a 16 bit serial word. In order to simplify the synchronization, the standard TV frame format was used. The digital word sent to the disc corresponds to

the first sixteen lines of a TV frame, each bit corresponds to one line. The code format is shown in Table III. The delay and integrate codes are set up on thumbwheel switches. Likewise, the correlate mode is set up on a thumbwheel switch on the front panel. A complete description of this circuit is given in the Appendix.

TABLE III
CYCLE CONTROL LOGIC CODE FORMAT

Lines (1,8,9,16)	Blank
Lines (2,3,4,5)	Difference Delay Code (BCD) Seconds
Lines (6,7,10,11)	Difference Delay Code (BCD) Tenth Seconds
Lines (12,13,14)	Integrate Code
Line 15	Control Bit

3.0 OVERALL SYSTEM PERFORMANCE

The measure of system performance has to be based on the likelihood of finding a satellite with a given video signal to noise ratio, and the time taken to perform that function. While the P_D and P_f values give some indication of this, they by no means tell the whole story. For example, if the cursor generation P_D was 50 percent, that would imply that the cursor would appear on the monitor 50 percent of the time. For all practical purposes, this is as good as 100 percent in a semiautomatic system and almost as good in a fully automatic system. It is not until the P_D falls to about ten percent that a detection starts to be unlikely in either the automatic or semiautomatic system. In that range between ten percent and 50 percent, the time to detection increases non-linearly.

To get a good measure of what a likelihood of detection curve would look like would require large amounts of empirical data taken from field tests which is unfortunately unavailable. However, to ignore this P_D enhancement would be absurd when in fact that is the way the system does indeed operate. A conservative estimate of likelihood of detection would be to use the ten percent P_D point as a likely detection. Figure 25 shows the P_D versus S/N for the various correlation modes used. These curves represent the P_D for a given video S/N into the CFAR detector. In order to determine the S/N, the disc processor operating mode must be taken into account as shown in Table IV.

For example, if the video S/N were 6dB, and the integration mode were eight frames, the detector S/N would be approximately 11dB. While

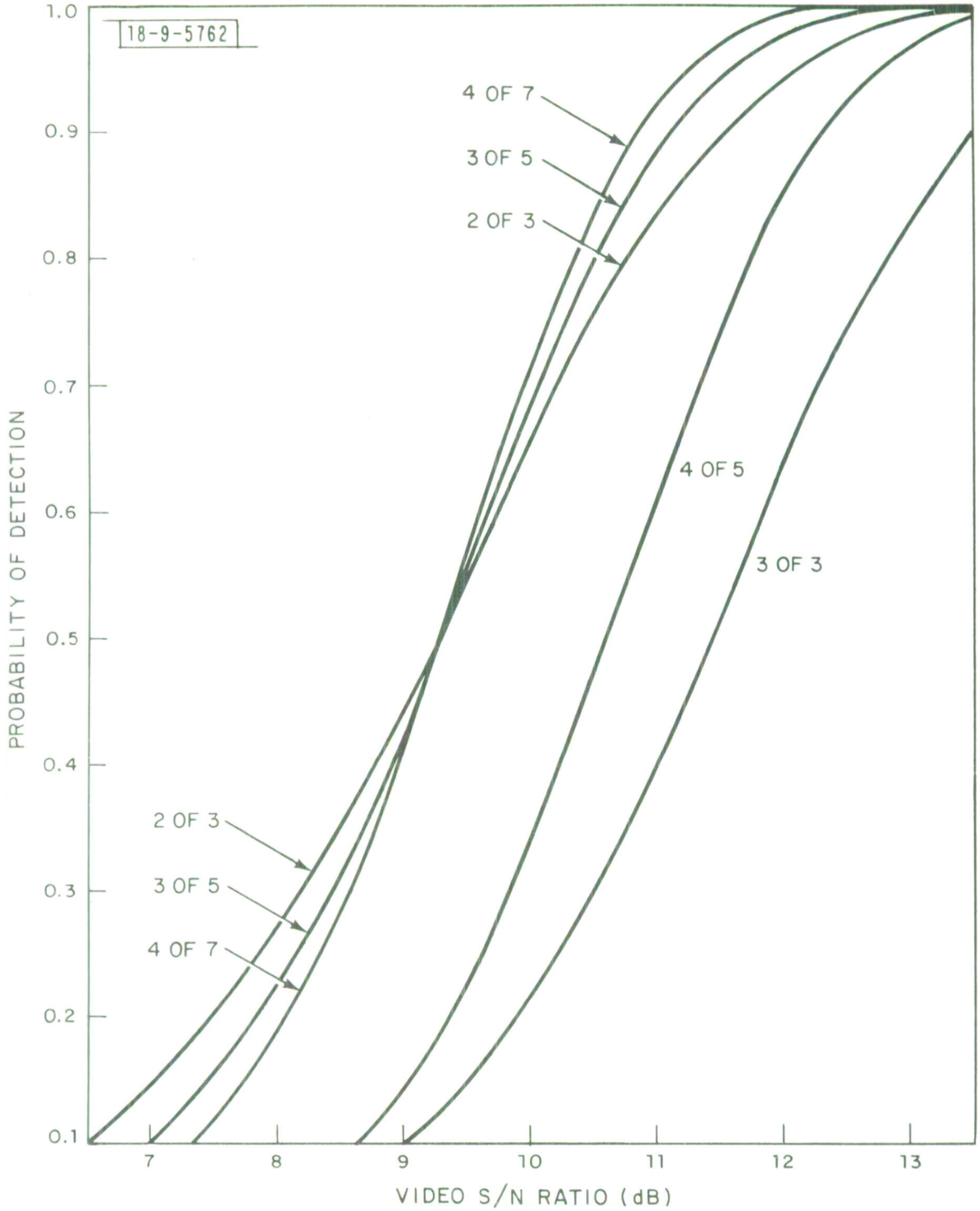


Fig. 25. Calculated probability of detection vs signal/noise.

TABLE IV

Camera Video	S/N
Difference Loss	-3 dB
Integration Gain	$(\mathrm{Log}_2 n)$ 3dB
Mismatch Loss	-1dB
Detector (S/N)	Video S/N -4dB + $(\mathrm{Log}_2 n)$ 3dB

the description of this processor has scrupulously avoided any discussion of the sensor except in the most general terms, one note of caution should be mentioned. Most sensors are power detectors, i.e., the output of the sensor varies linearly as the change in luminous flux per unit time. Therefore, a change in image intensity of 4dB (one stellar magnitude) would cause a change in video of 8dB.

4.0 FIELD TEST RESULTS

Laboratory tests were performed on the MTI system using an electronically simulated star field and satellites. The results of those tests indicated a good detection capability with an input signal to noise ratio as low as 0.7. This was accomplished with eight frames of integration and a correlation criteria of (3 of 5). The satellite velocities were from 1/2 synchronous to 2x synchronous in the simulated $0.8^{\circ} \times 0.6^{\circ}$ FOV. The range of NSB (night sky background) was varied from 10mv RMS to 100mv RMS. These results were consistent with the predicted performance and the system was shipped to the field site for a true environment evaluation.

On 9 February 1977 (Day 40 GMT) the system was set up at the GEODSS[1] site at WSMR. The telescope provided has a 31" aperture with an f/5 focal ratio which yields a 1.16° diagonal FOV on an 80mm focal plane. The camera[2] used an intensified SIT tube and had a 2:1 "Zoom" provision for increased sensitivity.

While many satellites were detected, only data on those which tended to show the limiting performance of the system were taken. For example, the detections listed in Table III-1 range from very steady

TABLE III - 1

DAY M/D	GMT D:H:M	SATELLITE File #	Mv	NSB	TE	FOV FF/Z	DET RATE	FA RATE
2/9	40:6:19	83564	13.5	20.4	0.30	FF	VS	L
2/9	40:6:50	8833	13.9	20.4	0.31	FF	VS	L
2/9	40:7:11	83567	14.1	20.1	0.31	FF	VS	L
2/9	40:5:55	83592	14.2	20.9	0.34	FF	VS	L
2/9	40:7:17	83542	14.2	20.3	0.31	FF	VS	L
2/9	40:6:44	83539	14.5	20.4	0.31	FF	S	L
2/9	40:7:32	83560	14.6	20.1	0.37	FF	S	L
2/9	40:6:34	83560	14.8	20.4	0.37	FF	S	L
2/14	45:7:45	83501	15.4	21.7	0.23	FF	S/0	L
2/14	45:5:14	83502	15.5	21.7	0.22	FF	S/0	L
2/14	45:8:38	83507	16.3	21.7	0.25	Z	S/0	L
2/9	40:7:40	83502	15.3	20.1	0.30	Z	S/0	M
2/14	45:5:03	83502	15.5	21.7	0.22	FF	0	M
2/14	45:8:19	83512	15.2	21.7	0.25	Z	0	M/H
2/9	40:7:45	83501	15.3	19.9	0.30	Z	0	H
2/14	45:4:23	83501	16.0	21.7	0.23	FF	0/R	H
2/14	45:7:21	83513	15.9	21.7	0.26	FF	VR	L
2/14	45:6:12	83512	16.9	21.7	0.25	Z	VR	H

FOV = Field of View; FF = Full Field; Z = Zoom

Mv = Stellar Magnitude

NSB = Night Sky Background in Stellar Magnitudes/sec^2

TE = Total Extinction

Detection Rating: VS = Very Steady; S = Steady; O = Often, R = Rate; VR = Very rare

False Alarm Rating: L = Low; M = Moderate; H = High

with a low false alarm rate to very rare with a high false alarm rate. Any detection achieved and catagorized as often was definately useful as an operator aid in finding the target. If a detection was rare it was sometimes useful, depending on the false alarm rate. That is, a rare detection with a moderate false alarm rate was marginally useful; a rare detection with a high false alarm rate was judged useless. Likewise, a very rare detection with a low false alarm rate was judged as only marginally useful.

The data on satellite magnitude, night sky background and total extinction is quantitative. The judgement of detection rating and false alarm rate is very subjective. However, the detection threshold is a rather abrupt function. If the probability of a CFAR threshold crossing is less than 1/2, the majority logic correlator rapidly drives the probability of detection down. Likewise, if the probability of a CFAR threshold crossing is greater than 1/2, the majority logic correlator rapidly drives the probability of detection up. From the small amount of data available, it is fairly clear that the system sensitivity is on the order of $15.5M_V$ with a NSB = 21.5 and falls rapidly as the satellite magnitude approaches $16.0M_V$.

The false alarm rate should not change for any given integrator mode. This is based on the assumption that the night sky background is a truly random phenomenon, i.e., the background is due primarily to "sky glow." The false alarm rate did change significantly over the period of observation and could be attributed to two factors:

1. Modulation of the background by high thin clouds.

2. High winds which physically displaced the telescope.

Both of these conditions were aggravated by the higher resolution "Zoom" mode. The reasons for this are fairly obvious. In full field, the area per resolution cell is four times that obtained in zoom. Therefore, in zoom the many more faint stars are resolved with an S/N above the level of the night sky background. That is, the lower resolution tends to produce a "noise whitening" of the background.

Figure III-1 shows the detection of three very slow satellites. Figure III-1(a) shows the difference field with no cursor, this is a typical display just before detection. The satellites can be seen quite readily as adjacent black and white dots in the difference field. Figure III-1(b) shows the detected satellites in the difference field. Figure III-1(c) shows the satellites in the "live" field. The cursor delay has been adjusted such that it surrounds the satellite in the "live" display. The cursor is displaced therefore in the difference field and the detected satellite tends to appear on the right hand edge of the box. Figure III-1(d) is a long time exposure of the same three satellites. This picture demonstrates the sort of false alarm rate and detection probability to be expected from this system. Figure III-2 shows the detection of a very faint synchronous satellite in a live field.

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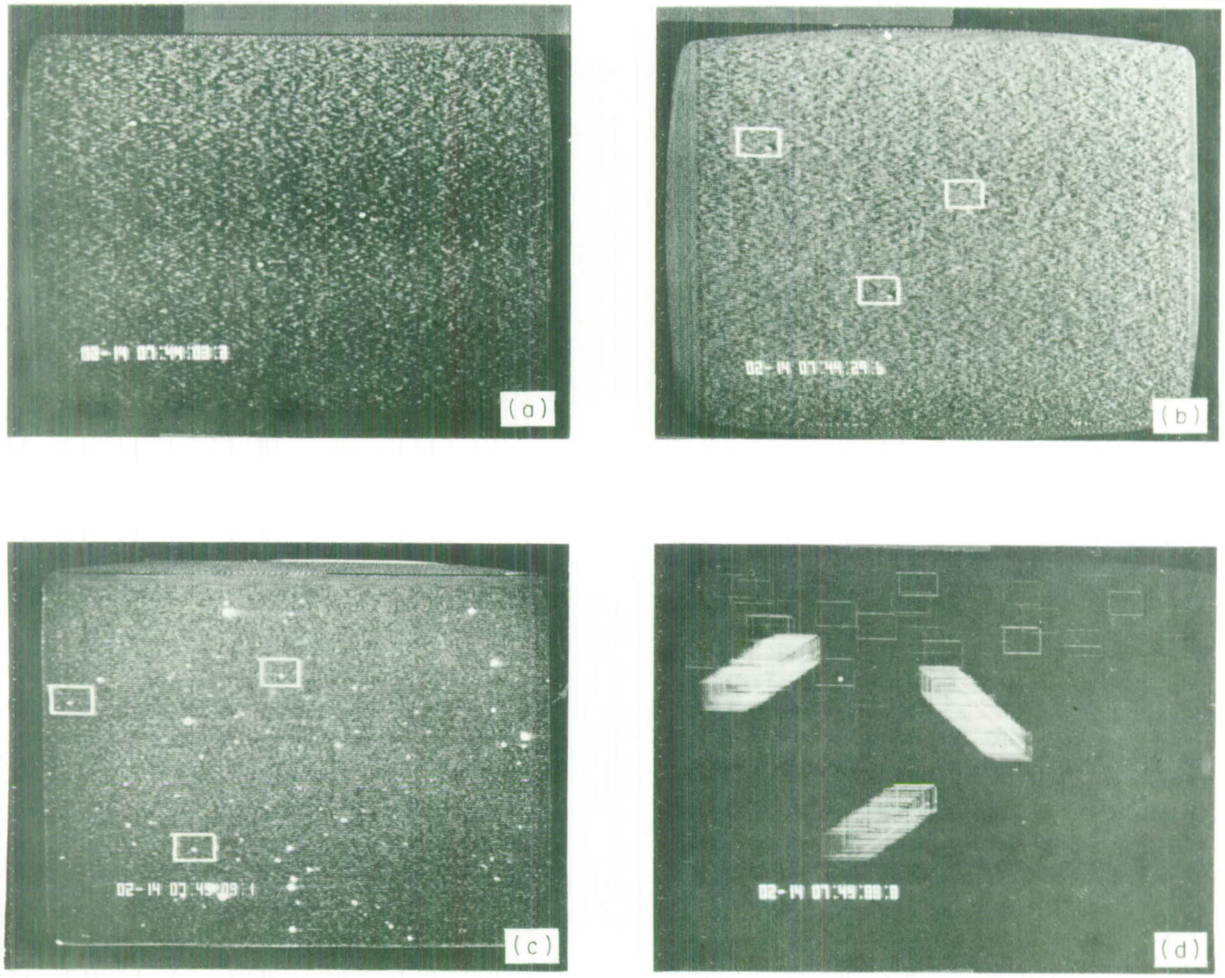

Fig. III-1. (a) Difference field (3 satellites with no cursors), (b) Difference field (3 satellites with cursors), (c) live field (3 satellites with cursors), (d) Time exposure of difference fields (3 satellites with cursors).

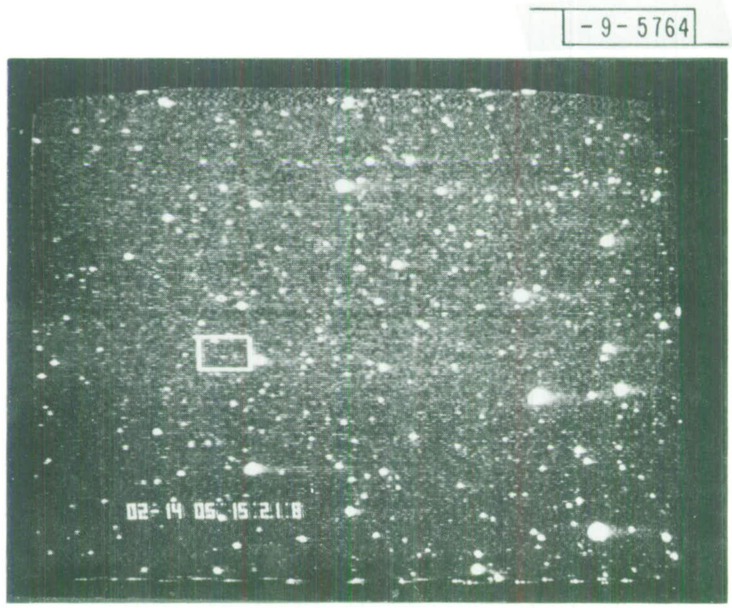

Fig. III-2. Monitor display of satellite detection in live field.

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2. R. Weber, "Predicted and Measured Detection Capabilities of the Lincoln ETS, Photon-Noise-Limited, Electro-Optical Systems," Technical Note 1976-9, Lincoln Laboratory, M.I.T. (26 April 1976), DDC AD-A025859/0.

APPENDIX I

NITH FINDER CIRCUIT DESCRIPTIONS

AI-1 CFAR DETECTOR M-25

The purpose of the CFAR detector is to set a threshold low enough into the noise to provide a high probability of detection in a low signal to noise ratio environment. The technique for accomplishing this is to set a threshold deep in the noise and count the number of threshold crossings and maintain that rate constant by automatic feedback. Figure AI-1 shows the overall block diagram for the detector circuit which is contained on one wire wrap circuit card.

Figure AI-2 shows how the detection scheme is implemented. Integrated Circuit #10 is a buffer amplifier which provides a 2x amplification of the difference video signal. The network following this amplifier bandpass filters the video and IC #7 is a voltage follower which acts as a buffer between the amplifier and IC's 6 and 18 the differential comparators.

The video from the camera is a function of the particular area of the sky the telescope points to. That is, if pointed in the direction of the milky way with the moon down on a clear night, the scene will be dense with stars. On the other hand, if pointed close to the horizon with the moon up on a hazy night, the noise background will be high and very few stars will be seen in the field. Because of this scene sensitivity, several steps have been taken to minimize its effect on automatic threshold setting. They are:

1. Automatic Gain Control of the video to maintain a nearly constant background noise level

2. Double Thresholding

3. Bright Star Blanking

The automatic gain control will be described in Appendix II. The principle behind double thresholding is to set a threshold deep in the noise for a very high threshold crossing rate and to offset a higher threshold from that for the desired rate. The reason for doing this is to make the threshold setting less sensitive to scene changes. If the number of threshold corssings caused by noise is much greater than those caused by scene effects such as incomplete cancellation of stars, this will be true.

The only assumptions made are:

1. The general probability density function of the noise is known.

2. The noise statistics are homogeneous across the entire field.

From the field test results, assumption one is probably correct and assumption two is correct only for high night sky background conditions.

The actual thresholding is implemented by differential comparitors (6) and (18) shown in Figure AI-2. Figure AI-4 shows the automatic threshold servo loop. Counters (38) (39) and (40) are set to maximum every sixteenth line and count down by the threshold crossings from the 10x CFAR threshold comparator. The most significant bit of counter (39) and all the bits of counter (38) are or'ed (negative) to form the most significant bit into latches (41) and (42). At the end of each 16 lines the data is transferred to the latches and held until the completion of

the next count interval. The most significant bit of the latch output is or'ed with the next three least significant bits and fed directly as a seven bit parallel word to the D/A converter (53). The output of the D/A converter is a "boxcar" type waveform whose level is inversely proportional to the threshold crossing rate. That is, the higher the rate, the lower the voltage and vice versa.

Integrated circuit (46) is an inverting amplifier and long time constant integrator. The DC gain of this circuit is 100x and the open loop line constant is 12.0 seconds. Potentiometer (55) is used to set the mean value of the threshold and (56) sets the differential ratio between the high and low thresholds.

The 5.1v zener acts as a variable resistance divider with potentiometer (56) such that a constant loop gain is maintained for all threshold levels. This is necessary because as the RMS value of noise decreases, this effectively changes the slope of $\Delta F/\Delta V$. Where:

ΔF = threshold crossing rate

ΔV = threshold voltage

This in turn increases the loop gain for low threshold levels, bringing the system to instability as the threshold approaches zero. The FD 777 diode and the 3.0v zener are used to provide the offset voltage for the 5.1 volt zener and prevent a latch up condition of the amplifier.

The overall loop gain of the system may be calculated at the maximum input noise level if the following assumptions are made:

1. The picture is quantized into 445 active lines and 234 active bins (pixels) per line

2. the noise has a Gaussian probability density function

3. the CFAR rate $\cong$ 6.0kHz or 200 threshold crossings per frame

4. the 10x CFAR rate $\approx$ 60kHz or 2000 threshold crossings per frame

where

V_{TH} = the 10x CFAR threshold voltage

F_N = the frequency of threshold crossings for a given noise voltage and threshold value

K_N = noise/voltage slope around an operating point = $\Delta F_N / \Delta V_{TH}$

A_o = $\Delta V_{TH} / \Delta F_N$ = open loop gain of the discriminator, i.e., the change in threshold setting for a given change in input frequency

$K_N A_o$ = closed loop again

$$\frac{K_N A_o}{1 + K_N A_o} = \text{closed loop accuracy}$$

$$1 - \frac{K_N A_o}{1 + K_N A_o} = \text{closed loop error}$$

$$F_N \left\{ 1 - \frac{K_N A_o}{1 + K_N A_o} \right\} = \text{CFAR error}$$

for example, assume:

V_N = 200μv = RMS noise voltage input

$V_{TH_{(10x)}}$ = 410μv = two percent threshold crossings

$V_{TH_{(1x)}}$ = 573μv = 0.2 percent threshold crossings

K_N = 1.52KHz/2μv

A_o = 102μv/1.52KHz

$K_N A_o$ = 612

Therefore, the accuracy of the 10x CFAR rate is within ±0.2 percent. However, the accuracy of the CFAR is much greater because of the difference in slope on that part of the density function, i.e., ±.0084 percent. In fact, the quantization error is larger than this and limits the accuracy of the 10x CFAR and the CFAR to ±.05 percent. The closed loop time constant is approximately 20 millisec. Therefore the settling time is 100 millisec or approximately three frames.

Figure AI-5 shows the schematic of the bright star detection circuitry. IC #3 acts as a shut clamp circuit which closes during the blanking interval, IC's 1 and 4 are buffers. IC #5 is a fixed threshold comparator which is set by potentiometer #59. The threshold is set at about 80 percent of the peak white amplitude to detect only bright stars, IC #32 is a shift register which quantizes the detections into horizontal bins and IC #33 selects the appropriate delay to compensate for processing delays on the disc. The shift register IC #30 is used to stretch the detection horizontally such that it overlaps the leading and trailing edges in the difference field.

Figure AI-2 shows the timing circuits for the CFAR detector. The 4.095MHz delay circuitry is provided to adjust the phasing of the detections to insure registration with the bins assigned in the correlator memory. The clamp circuit delay and generation places the clamp pulse in the blanking interval.

AI-2 CORRELATOR CONTROL BOARD

The correlator control board M-5 routes signals to and from the correlator memories, and provides the correlation of those signals. It also provides the timing cycles, the bright star blanking and the alarm function.

Figure AI-6 shows the circuitry for the bright star and overflow blanking. IC #1 has two line receivers used to buffer the CFAR and bright star detections. In gate #3 detections which are coincident, i.e., on the same resel location or on the same horizontal location from the previous line are blanked.

IC #29 is a multiplexer which switches on alternate lines such that the CFAR detections appear alternately on outputs 1Y and 2Y and the bright star detections appear alternately on outputs 3Y and 4Y. The outputs are written into memories #25, 26, 27, and 28 and are read out on the succeeding line. These read outs are demultiplexed in IC 38 such that the two outputs are the CFAR and Bright Star Detections from the previous line.

Gate #41 (pins 3, 4, 5) is used to blank CFAR detections which occur on the line previous to a bright star detection. The output (pin 6) is the CFAR detections one line delayed with blanking from the bright star detections on the same line and the two adjacent lines.

Counters #54 and 42 are reset during the vertical blanking interval and counts detections per field. When 128 detections are counted, any succeeding detections are blanked by the Q_D output of counter #42, this prevents the overflow of the correlator memory.

Gate #41 (pin 14) provides a burst of 4.095MHz clock which is used to clear memories (erase). This burst is summed with the CFAR detections such that it sets all memory locations to "one" in resel location (0, 0) prior to storing detections. It is also used in the same fashion for the cursor generator memories. The output of gate #41 (pin 10) is the composite of the CFAR detections and the clear memory function.

Counter 14 and 15 are used to count horizontal resel locations and are cleared during the horizontal drive interval. Flip Flop #10 toggles on the horizontal drive to provide the drive for the multiplexers.

Figure AI-7 shows the multiplexing scheme for the correlator memories. IC #22 sequentially sends CFAR detections to each of the memories. Counter #20 provides the encoding for the multiplexer by counting correlator sequence clock pulses. This clock rate is determined by the integration mode chosen, i.e., if no integration is used, the clock rate is 30PPS, if four frames of integration are used it is 7.5PPS, etc. The write enable gate allows only the first frame of detections following a clock pulse through the multiplexer.

The cycling of counter #20 is determined by the setting of the correlator mode switch on the master control panel by the load inputs. Thus, if the 2 of 3 correlation mode is chosen, the counter cycles on every fourth clock pulse. This provides sequential writing in memories one through four. When one memory is written into, the remaining three are read out into the line receivers 7a, 7b, 6a, 6b, 4a, 4b, 3a and 3b. The unused memory outputs and the memory currently being written into

are disabled by use of the strobe inputs to these receivers. The code for the strobe information is derived via multiplexer #17 and gates 32 and 16.

Gate #23 is used to start the cycling of counter #20 when a "disc full" signal is present and to detect when the cycle of this counter is complete. This signal then is used to light a lamp signifying that the processor is now "ready", i.e., it has sufficient information to generate cursors.

Figure AI-8 shows the correlator and the alarm circuitry. IC #19 is a "Read Only Memory" that has been programmed such that output #1 is high when any two inputs are high simultaneously. Output #2 requires three high inputs, output #3 four; output #4 requires five. These outputs are selected by data selectors #31 and 43 by the correlator mode switch information. The output of IC #31 is used to generate cursors on the basis of the correlation mode chosen. The output of IC #43 is one order higher than the correlation mode chosen, i.e., 3 of 3; 4 of 5; 5 of 7. This more stringently derived detection is used to drive the alarm circuit.

The alarm circuitry is very straightforward. The first half of IC #33 is a multivibrator which is triggered from the output of IC #43 during the "write enable" interval. If a second output from IC #43 occurs during the two seconds when the output of IC #33 is high, the second half of IC #33 is triggered. The two outputs activate IC #21 which provides both a flashing alarm lamp and an audio alarm by providing return paths for a lamp and a "Sonalert."

AI-3 CORRELATOR MEMORIES M1, 3, 7, 9

The circuitry for the correlator memories is shown in Figures AI-9 (horizontal) and AI-10 (vertical). There are two complete memories per card and four cards for a total of eight memories. The two memories share a common resel counter which provide eight bits horizontal and eight bits vertical. Detections are stored as 16 bit words corresponding to the resel locations and a total of 256 words may be stored, but no more than 128 words per field. Since both memories are identical, only the "odd" memory circuitry will be used for IC reference locations.

At the start of the "write cycle," during the vertical retrace interval, horizontal resel counters #27 and 33 and vertical resel counters #35 and 29 are cleared and held clear. Address index counters 2 and 14 are also cleared, but not held low. During this blanking interval, a burst of clear memory pulses appear at the "W-odd" input of IC #32. These pulses activate the 93410 RAM's (Random Access Memories) at the WE (Write Enable) input and trigger "one shot" #1. The output of this "one shot" is "ored" through gate #25 (pin 6) to provide the clock for the address counters #2 and 14. The counters advance to the next location, thus all address locations are stored with a "1" at resel location "0."

At the end of the vertical blanking interval, the resel counters are clocked by the 4.095MHz (horizontal) and the H-DR (Horizontal Drive) (vertical counters). The first CFAR detection initiates the WE to the 93410's and the resel count which appears at the DIN (Data Input) to the 93410's is stored as a 16 bit word in location #1. Successive detections are stored in successive locations in memory.

At the start of the "read cycle," the resel counters are again cleared but no "clear memory" appears. At the end of the blanking interval, the first word stored in memory appears at the outputs of the 93410's and at the inputs to the digital comparators 10, 5, 17, and 22. The alternate inputs to the comparators are connected to the resel counter outputs. When the word stored in memory is coincident with the horizontal or vertical resel count, and A = B output of the comparator goes high. Both horizontal comparator 22 and vertical comparator 5 are "anded" in gate 25 (pin 3) and drive both the output multivibrator 1 and is "ored" through gate 25 (pin 6) to advance to the next memory location. This sequence proceeds until all memory locations have been read and begins again at the start of the next frame.

Flip Flop 49 toggles on the vertical drive pulse thus generating a square wave which corresponds to the odd and even field. This square wave is used to partition the memory into two parts one for odd and the other for even field detections. This is accomplished by driving the "A7" address inputs of all the 93410's with this square wave. In order to insure that the square wave maintains the same phase relationship to the odd and even fields, the flip flop is reset by the odd field pulse.

AI-4 CURSOR GENERATOR M-13

The cursor generator circuitry is shown in Figures AI-11, 12 and 13. Figure AI-11 is the interface and provides the necessary timing signals to the Cursor Generator. The cursor is generated on alternate frames and the detection locations stored on the opposite. This is accomplished by dividing the OFP (Odd Field Pulse) by two and thus generating a read/write square wave.

Because the buffer memories used in the cursor generator are inverting, and because a timing offset is required between read and write, separate read write clocks are provided. These clocks drive the resel counters up on write and down on read. Counting down on read provides the equivalent of a complimentary or inverted output. It also provides an advance by loading the counter to some preset number before read and clearing the counter before write. These UP/DN clocks and load/clear signals are generated in gates 2 and 16 and the logic is self explanatory.

Figure AI-12 shows the circuitry for the cursor generator memory. The 3101A RAM's will store eight detections per frame. During the write cycle, multivibrator 15 is driven by the correlator output which is a composite of the correlated detections and the "clear memory burst." The memory is cleared in the same manner as that described for the correlator memories.

Successive detections are written into memory as sixteen bit words which correspond to the up counting resel counters. Because these words correspond to the resel locations of the detections, they can not simply

be "read out" with the same timing as a cursor start signal. Therefore, the counters are advanced by loading to 01101111 on both H and V before counting down. This effectively gives a nine element advance when compared to the complimentary number stored in memory. The output of the comparators is handled virtually the same as the correlator memory and used to provide a "start cursor" pulse.

The circuitry for the cursor generation is shown in Figure AI-13. There are four individual cursor generators which are triggered sequentially and can run simultaneously to allow for multiple targets and false alarms. Once a cursor has been generated completely, that generator assigned to it is now ready to start a new cursor so that as many as eight cursors per field or sixteen per frame are possible.

IC #31 is the input multiplexer for the first two cursors. If a negative going start pulse appears at input A_o, outputs 0_1 and 0_2 go low, loading counters 32, 44, and 56. If a second cursor start signal should occur before the generation is complete, outputs 0_3 and 0_4 go low to start a second cursor. If a third start signal should occur before either is complete, output 0_5 will go low to trigger multiplexer 35.

When counters 32, 44 and 56 are loaded, output 0_1 of IC 55 goes low thus enabling the counters. Outputs 0_2 and 0_3 of IC 43 go low for the first 16 resel counts following the cursor start signal. The gated clock provides 234 clock pulses per line by providing a dead space during the horizontal drive interval. Counters 32 and 44 are programmed

for a modular 234 count through the load inputs with the feedback from 0_1 of IC 43 via $A_2/0_2$ of IC 31. Counter 56 is clocked each time a cycle of 234 resels is complete, thus providing a line count. Output 0_2 of IC 55 is low for the first and sixteenth line of the count only providing an input to IC 43 on A_8.

Output 0_3 of IC 43 goes low for the first sixteen elements of every 243 thus providing an area gate starting nine elements before and nine line above the detection. Output 0_2 goes low only for the first and last elements of the area gate on lines 2 through 15 and for all elements of the area gate on lines 1 and 16 thus providing a box which surrounds the detection.

When the cursor generation is complete, output 0_1 of IC 55 goes high thus disabling the counters until the next "start cursor" pulse. The outputs of all the cursor and area gates are "ored" (negative) in IC 33 to be mixed with video in the video amplifiers.

AI-5 INTERFACE LOGIC M-11

The purpose of the interface logic is to provide synchronization with the Disc Recorder; generate control signals and provide basic timing for the correlator. The schematic for this logic circuitry is shown in Figures AI-14 through AI-19. Standard TV synch signals are generated from a clock derived from a synch track permanently recorded on the disc. The camera and the correlator are hard locked to these synch signals to insure almost perfect registration with the video recorded information throughout the system.

Figure AI-14 shows the cycling control logic circuitry. Data is sent to the disc via shift registers 21 and 9 in a 14 bit serial code. To simplify encoding and decoding the first 14 lines following the "odd field pulse" are used as data space. The code format is shown in Table AI-1.

The data inputs to the shift registers are provided by thumbwheel switches located on the correlator master control panel. When in the correlator control mode this data provides information on the difference delay time and the integration mode selected. When in the disc control mode or when the disc/correlator cable is disconnected, the disc operates as a "stand alone" system and there are another set of thumbwheel switches located on the disc module nest which perform the same functions.

Counters 32 and 34 are modular-m programmable from the integrate mode information provided by ROM33. The purpose of these counters is to divide the frame rate by the number of frames integrated and generate

TABLE AI-1

CODE FORMAT

TV Line	Function	
1	Difference Delay MSB	
2	" "	1.0 SECS
3	" "	BCD CODE
4	" " LSB	0-4
5	" " MSB	
6	" "	1.0 SECS
9	" "	BCD CODE
10	" " LSB	0-9
11	SINGLE/DOUBLE Int $(X_1)(S_3)$	
12	Int Code (X_2)	
13	Int Code (X_3)	
14	LOC/REM BIT	

the correlator sequence clock and the write enable gate. The "disc full" signal when low holds the counters in the load state. When the "disc full" signal goes high the counters are free to count at a normal rate.

Figure AI-15 shows the "pipeline delay" timing circuit. The purpose of this circuit is to sense the start of sidereal track and then count out the time required to fill the operating tracks of the disc. This is required to prevent false alarms caused by the subtraction of two different scenes. There is an additional delay, programmable from one to six seconds to allow for telescope settling after the sidereal track signal is received.

Timer 36 provides the delay just mentioned. When the sidereal track signal is high, the output of opto-isolator (8) is low. This holds counters 44, 10 and 23 in the load state, thus inhibiting them. When the sidereal track signal goes low or the cable is disconnected, timer 36 is triggered. At the completion of the cycle, the timer output goes low and the output of gate 35 (pin 13) goes high, thus allowing the counters to cycle normally. Counters 10 and 23 count down from the programmed number in 0.1 second and 10 second increments respectively. When the count reaches zero, the minimum/maximum output of 23 goes high, thus generating the "disc full" signal and inhabiting further counting by the active low input enable of 10.

Figure AI-17 is a schematic of the isolated line receivers used to buffer the synch signal from the disc. Line receiver (1) receives the

2.0475MHz clock signal from the disc via a twisted pair shielded cable. Multivibrator 13 converts the 2.0475MHz to 4.095MHz by generating a pulse at each positive and negative transition. These pulses are summed in gate (2).

Multivibrator 15 is used to regenerate the Horizontal DR pulse. This is necessary to insure that the pulse width will gate out exactly the correct number of pulses of clock for the resel counters. There is an interval clock in the system for test purposes. When the switch on the master control panel is switched to correlator synch, this automatically switches the "T" synch outputs to these internally generated timing signals.

Figure AI-18 shows the delay code signals. Because the disc processor has an inherent delay which varies with the integration mode chosen, it is necessary to compensate for this when superimposing a cursor on the video display. Figure AI-19 shows the circuitry for the internal synch generation. Crystal oscillator 30 provides the basic clock for the system. The synch generator 19 provides all the standard synch signals with no additional circuitry required. These synch signals are at standard TTL level as they are to be used internally only.

AI-6 CONTROL PANELS AND WIRING LISTS

The layout and wiring for the control panels is shown in Figures AI-20 through AI-38. The wiring lists are Figures AI-39 through AI-43. The module nest wiring shown in Figure AI-43 reads from left to right, i.e., if a wire starts anywhere, its destination is always to the right. The symbol (∞) signifies the final end point of a chain of connections. An (X) symbol signifies a twisted pair connection, an (o) symbol signifies a coaxial connection. Voltages and signals to and from the module nest are called out by their designation.

APPENDIX II

DISC RECORDER MODIFICATIONS

The Video Disc Recorder was received in our Laboratory on 14 April 1976. Since that time, a series of modifications have been incorporated to upgrade the performance. In addition to these modifications, several more basic changes will have to be made before the unit is suitable for field application. The following is a summary of all these changes.

AII-1 VIDEO PROCESSING AMPLIFIERS

The incoming video signal from the camera is first sent to a processing amplifier which clamps the signal at TV line rates to reduce any hum introduced by pickup from the long cables from the camera to the disc. The processing amplifier then removes the synchronization pulses before recording since this is redundant information and if recorded would reduce the maximum available signal to noise by approximately 3 to 5dB. The signal is the AGC amplified to maintain a constant video noise level and fed to the first modulator where the voltage waveform is converted to the FM carrier to be recorded.

There are a number of possible system configurations, i.e., differencing, single integration of up to eight frames, doubling integration of up to forty-eight frames.* Because of this, three video processing amplifiers with switching both at the amplifiers and the modulators was provided. In block diagram form this allowed for all that we had requested.

Examination of the video signals from the processing amplifiers revealed that there was considerable pickup of 2MHz system clock signal

*The second integration section has been detected because of the limited application and to improve reliability.

which was clearly visible on the monitor. In addition to this, there was considerable non-correlated hash from the modulators on the video which did not appear on the monitors, but did introduce a cross talk between channels. All three video channels were provided with clamp circuits which was clearly a mistake. Clamping after record and playback only served to clamp record/playback noise which occurred during a blanking interval to be clamped across an entire line.

About a week and a half was spent attempting to minimize the crosstalk and pickup. It became increasingly clear that while it might be possible to get such a configuration to work, it was not the most straightforward or expedient solution to our problem. What was required was good isolation between all inputs and outputs which meant many more video amplifiers and double pole/double throw switching which would insure isolation by minimizing common mode coupling.

A simple unity gain amplifier with 75Ω input and output impedances was designed to be incorporated on two 16 pin component carriers. Since this was a new design, provision was also made for synch and cursor insertion for our convenience. Fifteen of these amplifiers were built to provide the outputs for the three modulators, two monitors, two outputs to the CFAR detector and correlator and internal system input/output isolation. These amplifiers are contained on two modules along with the input clamp circuit and synch stripper.

Figures AII-1 and 2 show the video amplifier circuit. The x2 video amplifier shown in Figure AII-1 is designed such that with pins 16, 8, 9 and 10 grounded the input impedance is 75Ω and the voltage gain is x2.

With pin 16 ungrounded, the input is a very high impedance and thus may be paralled with other amplifiers providing multiple outputs. Pins 8, 9 and 10 may be used for summing of signals such as cursors or synch or for a DC offset control.

The driver amplifier shown in Figure AII-2 has unity voltage gain and an output impedance of 75Ω. When terminated, the voltage gain is 1/2. Thus when used in combination with the x2 video amplifier the overall voltage gain is unity with input and outputs terminated in 75Ω.

Figure AII-3 is the video clamp circuit. This is a standard diode shunt clamp. When the clamp pulses are applied, the transistors are turned on thus forward biasing the diodes. Since the forward voltage drops of the diodes are equal and opposing, they cancel and the voltage from pin 9 to pin 11 is zero. This acts a low impedance path from pin 9 to ground, thus clamping the video waveform by charging the 6800pf capacitor to the offset voltage on the video. Clamping occurs on the "backporch" of the synch and is used primarily to minimize hum and DC offset on the video.

The video noise AGC circuit is shown in Figure AII-4 and 5. This circuit is intended to maintain a constant background noise level to insure phoron noise limited operation. The feedback network is a high pass video filter, detector and amplifier which controls the gain of a video amplifier. The high pass filter will pass the RMS noise, but not the shading and is relatively insensitive to star populations in the scene. The detector is a simple shunt diode followed by a low pass filter and a high gain operational amplifier.

The gain of the video amplifier is controlled by a voltage controlled resistance (VCR) which shunts the input emitters of a differential pair. When the VCR is in the high resistance state, the gain of the video amplifier is minimum and the throughput gain of the overall network is adjusted for unity by means of the input range potentiometer. As the VCR decreases to the low resistance state, the video amplifier gain increases. In order to minimize the effects of pedestal and shading amplification, a high pass network is in series with the VCR to increase high frequency gain faster than low frequency components.

There is a DC feedback loop included to prevent latchup with a high noize level input. With a scene change from low to high noise level, such as caused by moving the telescope towards the moon, the AGC will respond too slowly to prevent severe clipping of the noise. Without DC feedback, this would tend to reduce the noise in the feedback thus increasing the gain and the clipping until the video amplifier was saturated.

The configuration of the video processing distribution amplifiers is shown in Figures AII-6 through AII-10.

AII-2 VIDEO DISTRIBUTION

A video switching module which provides DPDT switching of all coaxial video signals and 75Ω termination of all unused signals was also designed. This allows five operating modes: Difference and Double Integration; Difference and Single Integration; Difference; Single Integration; and Double Integration. Two monitor switches are also provided. The first monitor may display "Live Input Video;" "Difference Video" and "Processor Video" all with cursor and synch inserted. The second monitor may display "Live Video;" "A-Video;" "B-Video;" Difference-Video;" "Integrator #1 Video" and "Integrator #2 Video". This monitor is intended for diagnostics and contains synch but no cursor.

The configuration of the video switching unit is shown in Figures AII-11 through AII-16.

AII-3 MODULATORS

The modulators convert the video voltage to frequency modulated carrier. Black level is 11.5MHz and peak white 16MHz. Since the video bandwidth is 4.5MHz, the modulation index is unity and therefore a high signal to noise ratio is required to maintain fidelity.

For recording, the FM carrier is divided by two and the information is carried in the positive and negative transitions of the half frequency square wave. On playback, the system is bandwidth limited by the head response and the output is a sinusoidal waveform of very low level compared to the modulating signals. Since all the information is contained in the zero crossing of this low level signal, it is extremely sensitive to contamination by crosstalk from the write signal or any distortion in the read channel which would perturb the phase of this signal.

The system as designed had separete Read/Write amplifiers for each recording head. Each Read/Write amplifier contains an input flip flop for dividing the FM carrier by two. This flip flop is enabled only during the write cycle and the head winding is switched from read to write by two sets of diodes which connect it either to the write drivers or the read amplifier. The read amplifier has a gain of approximately 100 to provide an output signal of 1.0 volts P-P during the read cycle.

Contamination of the read signals by the write signals was evident and attempts to solve this by additional shielding and grounding proved fruitless. The effects of this crosstalk could be minimized by carefully adjusting the heads for optimum output and dressing the leads to minimize

pickup. However, the system remained very sensitive to lead dress and the performance would seem to vary as a function of operating time, temperature and slight variation in the positions of cables.

Therefore, the following changes were made: The modulators were moved from the module nest and put in a shielded box on the disc housing. A multiplexer which switched the modulating signal from head to head was provided in the same box. Therefore, the modulator signal is present at the R/W amplifier terminals only during writing, thus eliminating the cross coupling at the amplifier and associated board wiring.

A separate sample from the modulator was attenuated 20dB to simulate the "A" channel. The "A" channel which consisted of two fixed heads alternately reading and writing was eliminated. The purpose of this channel was to provide a similar channel for subtraction such that any non-linearities introduced during record/playback would be duplicated in both channels.

Most of this intent was preserved by coupling the output of the modulator directly to the "A" channel demodulator through a series of delay lines. This eliminated the crosstalk between the A channel write and B channel read which was caused by the close proximity of heads and Read/Write amplifiers. There is no apparent degradation in performance caused by bypassing the recording process and virtually all the read/write crosstalk has been eliminated. Elimination of these heads also gives the added benefits of simplicity and improved reliability.

The schematic for the modulators is shown in Figure AII-17.

AII-4 DEMODULATORS

The purpose of the demodulators is to amplify the read signal from the heads to the point of hard limiting and to extract the zero crossing information. The original design was quite complicated and provided for frequency and delay equalization. From a theoretical point of view, this is all necessary since the recording process is severly non-linear with respect to frequency.

However, from a practical point of view the complexity far outweighed its value. The high gain required in the limiting amplifiers tended to make them inherently unstable and a long chain of amplifiers with unshielded tunable inductors further aggravated this situation. With the module on the extender and one cover removed, it was impossible to keep the demodulators from oscillating and thus impossible to adjust the equalization. With the covers in place and the module inserted, the adjustments are inaccessible.

To determine empirically how important the equalization was, the read signals were coupled directly to the final limiting amplifier, thus by passing approximately 75 percent of the demod circuitry. Clearly, the performance was drastically improved. No noticeable edge effects due to a lack of frequency equalization could be detected and therefore all demodulators were modified accordingly.

In order to minimize crosstalk, the cables from the read/write amplifiers to the demodulators were changed from single ended coax to twisted pair shielded. In order to do this, the output circuitry on the R/W amplifier was eliminated and the differential output of the μA 733 was AC coupled to a balanced attenuator network.

In order to adjust delay between each channel, standard TTl delay lines with 5 nanosecond taps are provided at the output of each demodulator prior to demultiplexing. The overall system jitter is on the order of 60 nanoseconds P-P, and a 5 nanosecond resolution is more than adequate.

The output of the demodulators is a square wave with both the positive and negative transition corresponding to the positive transitions of the original modulating frequency. With a steady state flat background, this square wave should be perfectly symmetrical, if it is not, distortions in the video signal reproduced will result. Non-symmetry can be produced in the recording by an imbalance between the erase flux and write flux which must be carefully biased with respect to each other. It can also be introduced by coupling from output to input of the demodulator which tends to distort the read signal, or it can be caused in the limiter itself by internal bias conditions. Most of the non-symmetry has been eliminated and the performance in this respect is adequate.

The outputs of the demodulators are coupled to a demultiplexer which selects the head currently reading and thus provides a single continuous output. This output is then coupled to an edge selector which generates a 35 nanosecond pulse at each transition. This pulse train is then amplified and low pass filtered, and the output of the low pass filter corresponds to the original video waveform with the corresponding delay between the record and playback time. This delay is on the order of several seconds which makes the MTI function possible.

For MTI subtraction, both the A channel and B channel pulse trains are fed to opposite inputs of a differential amplifier before low pass

filtering rather than subtracting after filtering. This avoids a very critical phase equalization problem near the filter cutoff which would be virtually impossible to achieve in the fast cutoff filter which is required to eliminate the carrier from the video.

The original design used very large pulse amplitudes at the input of the filter to achieve a large video signal at the output of the filter. From an analytical approach, this is the optimum design since amplification after filtering introduces some noise into the system. However, the generation of these large pulses requires a large power bandwidth achievable only in discrete circuitry. The layout of this curcuitry is very critical and must be done with great care to avoid cross coupling. Unfortunately, not very much consideration was given to the layout. Transistors seemed to be scattered randomly around the board and long leads between them radiated into everything. As a result, the output video contained large amounts of high frequency carrier hash. This hash would tend to be rectified in subsequent circuits and the result was a background cross coupling which appeared on the monitor as a displaced image at a very low level which could not be subtracted and was very unpredictable in nature.

Therefore, this circuitry has been modified to a low level integrated circuit design with a much more careful arrangement of components. This requires amplification of these signals after filtering, but any noise introduced will be well below the system noise level. The demodulator circuit charges are shown in Figures AII-18 through AII-22.

AII-5 SYSTEM GROUNDS

In any large integrated system where many high and low level signals are piped around, either one or two basic philosophies are used for grounding. The first is to provide separate DC returns for each sub-assembly and a single "star-ground point." This minimizes common mode coupling by essentially isolating each circuit. The second approach which is generally not as good but most often used for reasons of economy and simplicity is to provide a very large, low impedance, ground plane. Because of the low impedance, cross coupling tends to be minimized in such an approach.

The original design tended to be a cross between the two approaches. All system inputs and outputs went through a common panel on BNC type connectors with non-isolated coax shields, thus tying all coax shields together. The other end of these coax shields were connected to the ground plane of the module where they either originated or terminated. Likewise, cables which were used to pipe video signals around were grounded in indiscriminate places which would change as the system configuration was changed. The output of the Read/Write amplifiers were sent through coax which was commonly grounded at the disc interface connectors and the Read/Write amplifier modules, then grounded again at the demodulator inputs. The modulator coax was grounded at the source, looped through isolated connectors at the disc interface connectors and the Read/Write amplifier modules, then grounded again at the demodulator inputs. The modulator coax was grounded at the source, looped through

isolated connectors at the disc interface, but was grounded at each individual Read/Write amplifier module. Separate DC returns from each power supply were provided but were common to all modules and tied to a common ground plane on each module.

Such a mix of approaches to grounding leads to difficult if not impossible common mode coupling. The following steps were taken to minimize the problems: All interface connectors on the back panel were changed to isolated BNC connectors. All the pulse type outputs to other equipment are to "Opto-Isolators" on the receiving end; video signals, whether switched or direct, are continuous in both center conductor and shield and terminated at both ends with shield connected to ground only at source and receiving end; and the disc assembly since it is so massive was considered to be a good ground plane. Therefore, each Read/Write amplifier was securely grounded to it. The modulator signals from the distribution box (new) are grounded separately on each Read/Write amplifier input. The distribution box is securely grounded to the disc assembly by mounting on it. The interface connectors for the output of the Read/Write amplifiers have been isolated from ground, thus tying the coax shields to ground only at the output of the individual amplifiers. The shield for this pair is connected at both the modulator source and the distribution box on the disc. The wiring changes are shown in Figures AII-23 through AII-32.

AII-6 CLOCK TRACK WRITING

The system operates from a separate clock track which is permanently recorded on the disc. If the disc is changed a new clock track must be recorded. In the original design there was no provision for recording a clock track. The technique is described in some detail in the Westinghouse Final Report BB-284. The circuitry for implementing it is shown in Figures AII-33 through AII-35. In addition changes to the Servo and Synch Generator module were required as shown in Figures AII-36 and 37.

AII-7 HEAD LIFTERS

At present, heads are always in contact with the surface of the disc. It is believed that, although not designed to do so, the heads actually fly a few microinches above the surface when the disc is rotating at its normal 1800 RPM. It has been noted that the head failures occur most often during start up and shut down, tending to support this theory. Further, tests made at Westinghouse using an ultrasonic transducer to pick up the high frequency sounds of head to disc scraping indicate the most severe wear occurs at low disc speeds. It has also been noted that when a head sits on one location on a disc, i.e., with the disc stationary, a dirty residue or footprint is left on that spot. It has also been noted by myself and confirmed by the head manufacturer that if left in one spot for several weeks, the head tends to become glued to the disc. This is believed to be caused by a very thin greasy deposit left on the disc by pollutants in the air. When the head sits in one spot for a long period of time, it tends to displace this deposit, like standing on the bottom of a muddy lake.

With so much evidence of failure caused by heads in contact with a slow or stationary disc, head lifters to prevent this would seem to be the only prudent approach to the head failure problem. The head manufacturer does make provision with a tab on the head assembly for head lifting and does make several different head lifters. Unfortunately, the mechanical design of the Westinghouse disc assembly did not lend itself easily to incorporation of these lifters and we had to design our own.

The head lifters operate by sensing the disc motor voltage which is proportional to disc speed. The head lifters are shown in Figures AII-38 and 39.

AII-8 DISC RUNOUT AND VIBRATION

I was present when the current disc was installed at Westinghouse. Although I witnessed the technique of measuring the height of the disc and its runout, the procedure used was so crude I could have little confidence in it. The measurements made at Westinghouse indicated an overall runout of 1.5 mils. When measured in our own lab with our own specially designed jig, the runout was measured at 6.5 mils. This could have a very serious effect on head life and performance in terms of amplitude modulation of the signal.

It has been found that this large runout is not caused by a non-flatness of the disc, but a non-perpendicular mounting between the disc and the motor shaft. Very careful shimming of the mounting reduced the overall runout of the disc to less than ±1 mil.

AII-9 JIGS AND FIXTURES

For installing a new disc and aligning heads, many mechanical jigs and fixtures had to be constructed as described below.

Figures AII-40, 41, 42 and 43 show the disc height and runout gauge. This has a teflon tipped screw which rests on the disc to measure overall runout. The resistance of the sensor varies as a function of position. With the readout provided, the resolution is ±.01 mil which allows for very precise measurements.

This same device is used to measure vibration by mounting it between the disc housing and the shock absorber cross member. The sensor is driven with a constant current power supply and the voltage across it which corresponds to the peak to peak displacement is measured on an oscilloscope.

Figures AI-44 and 45 show the head height adjustment jig. This is an alternate technique to the one described in the Westinghouse final report. The head height is adjusted on the mounting block such that when the mouting block is mounted on the module plate, the head to disc spacing is 0.197 inches.

Figures AII-46 and 47 show the head alignment test jig which is used to check the head landing. This jig simulates the disc casting and the surface of the disc.

Figures AII-48 and 49 show the head pressure gauge which measures the contact pressure of the head and feet on the surface of the disc.

Figure AII-50 shows the top half of the disc casting with a centerpunch jig mounted in the middle. This jig is used to check radial alignment of the heads with a divider.

Figure AII-51 shows a plastic overlay jig that was made as an alternate method of checking radial head alignment. There are four alternating colors in scribed lines which greatly ease the problem of head alignment. All four heads in a group may be checked simultaneously and the tracking of head and feet is much more precise than with the divider method described in the Westinghouse final report.

APPENDIX III

SIMULATOR

In order to test the Video Disc Recorder and the CFAR detector and correlator in the laboratory, an electronic simulator was designed and built. The simulator provides a reasonable number of bright stars, i.e., full amplitude and occupying more than one resolution cell; one dim star per line with four different amplitude levels; a variable background noise level; a satellite whose velocity direction and amplitude are variable.

The intent of the simulator was to generate video waveforms as close as possible to "real world" conditions. The use of tape recordings was considered, but discarded because of the difficulties in maintaining the time base stability required; hum and shading introduced in the recording process and the inability to independently vary any parameter.

Figure AIII-1 shows the synch and timing circuits. The simulator is normally operated as a camera would be, i.e., from the disc synch and timing signals. An interval synch generator has been provided for test purposes or for use with other systems.

Figure AIII-2 shows the circuitry for the satellite generation. Operational amplifier 26 is a long time constant integrator which is used to generate a slow sawtooth. The period of the sawtooth is equal to the time for a satellite to traverse one field of view and is adjustable in five steps from 1/3 synchronous velocity, 5 sec/sec to 3x synchronous velocity, 45 sec/sec for an equivalent 1^{o} FOV.

Operational amplifier (48) is used as an inverter to provide the opposite direction in sawtooth voltage. The satellite sawtooth is summed with a composite of horizontal and vertical sawteeth in the satellite rotation network. A full rotation of the potentiometer will cause the satellite velocity vector to rotate through one quadrant. By rotation of S_1 all four quadrants may be selected. The satellite velocity will remain constant regardless of the vector direction chosen.

Comparator 40b compares the composite ramp to either a positive or negative going vertical ramp depending on the direction chosen. When the two ramps are equal, multivibrator (41b) fires generating a 63a sec (one line) pulse, this happens once per field. Comparator (41a) compares the inverse of the composite ramp to either a positive or negative going horizontal sawtooth. This generates a pulse on each line from multivibrator (41a). Gate (30) "ands" these pulses (negatively) and the output pulse corresponds to the satellite video.

Figure AIII-3 is the circuitry for the star field generation. Inputs Y_o through Y_7 correspond to the line count. IC's 162 are ROM's which have been programmed for a bright star area code on each line. ROM 1 is the odd field and ROM 2 is the even field code. The outputs of these ROM's are a 4 bit code which drives a D/A converter. The output of the D/S drives opposing amplifiers such that as one increases, the other decreases. Therefore, at code (0000) there is no differential voltage between the two outputs and at code (1111) there is a maximum differential voltage.

The output of these voltages is summed with the bright star position code and fed to comparators 15 and 16. The other side of the comparators has a horizontal sawtooth applied. Depending on the differential voltage on the comparators, one will trigger before the other. Exclusive OR 14 translates this to a pulse which corresponds to the bright star video voltage.

The dim star position uses information from ROM's 6 and 8 to provide 256 possible locations. Comparator 9 compares the dim star position voltage to the horizontal sawtooth and generates a 250 nanosecond pulse on each line. ROM 11 generates the dim star amplitude code. THe dim star amplitude modulator is shown in Figure AIII-4.

Figure AIII-5 shows the video mixing circuit. Figure AIII-6 shows the video noise source. In order to simulate the mean value of the noise, the noise has a DC component which is always proportional to the RMS noise level. Both this noise and the DC pedestal are blanked during the blanking interval as they would be from the camera.

Figure AIII-7 is the module nest wiring for the simulator.

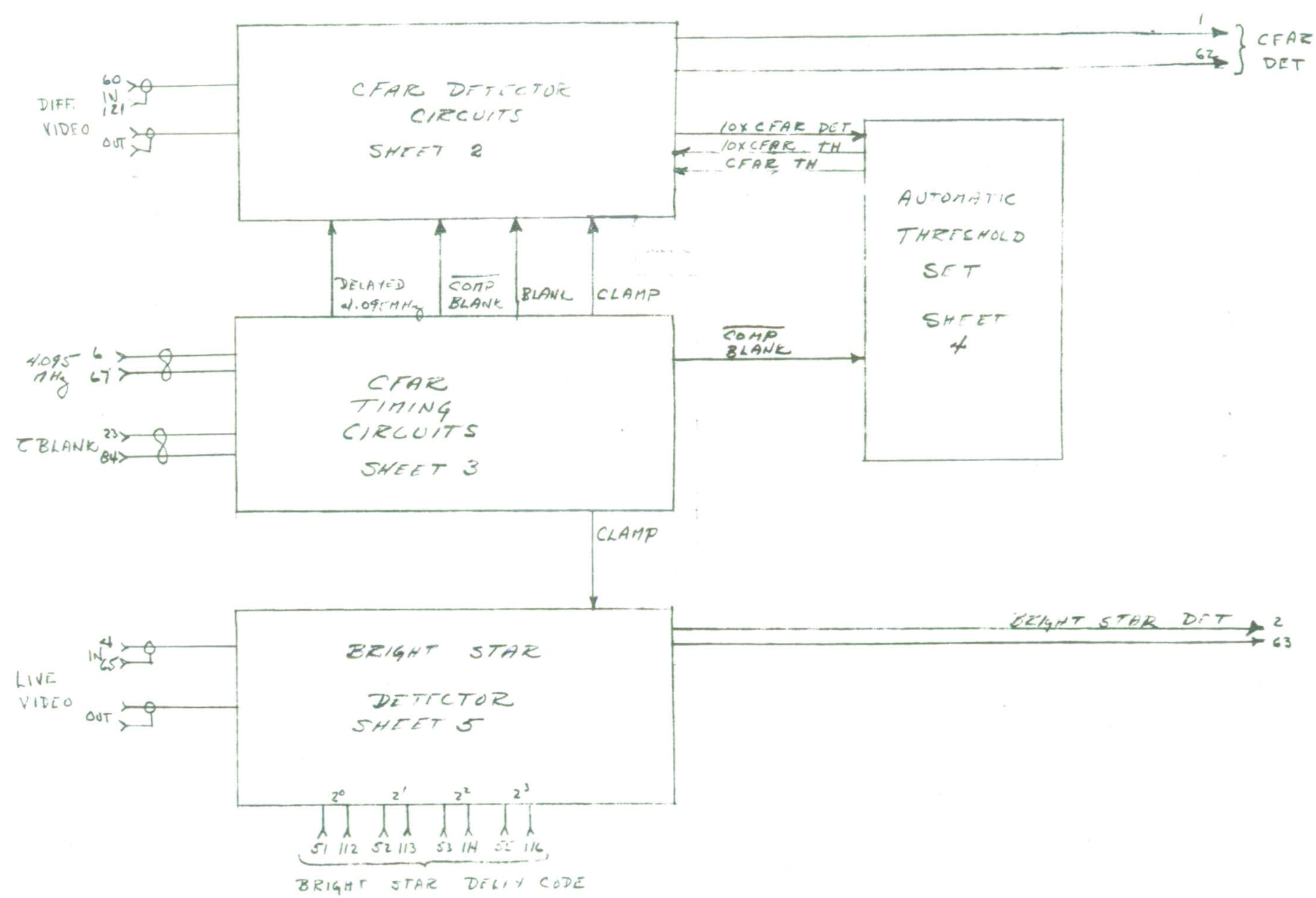


Fig. AI-1. CFAR Video Processor (Sheet 1 of 5).

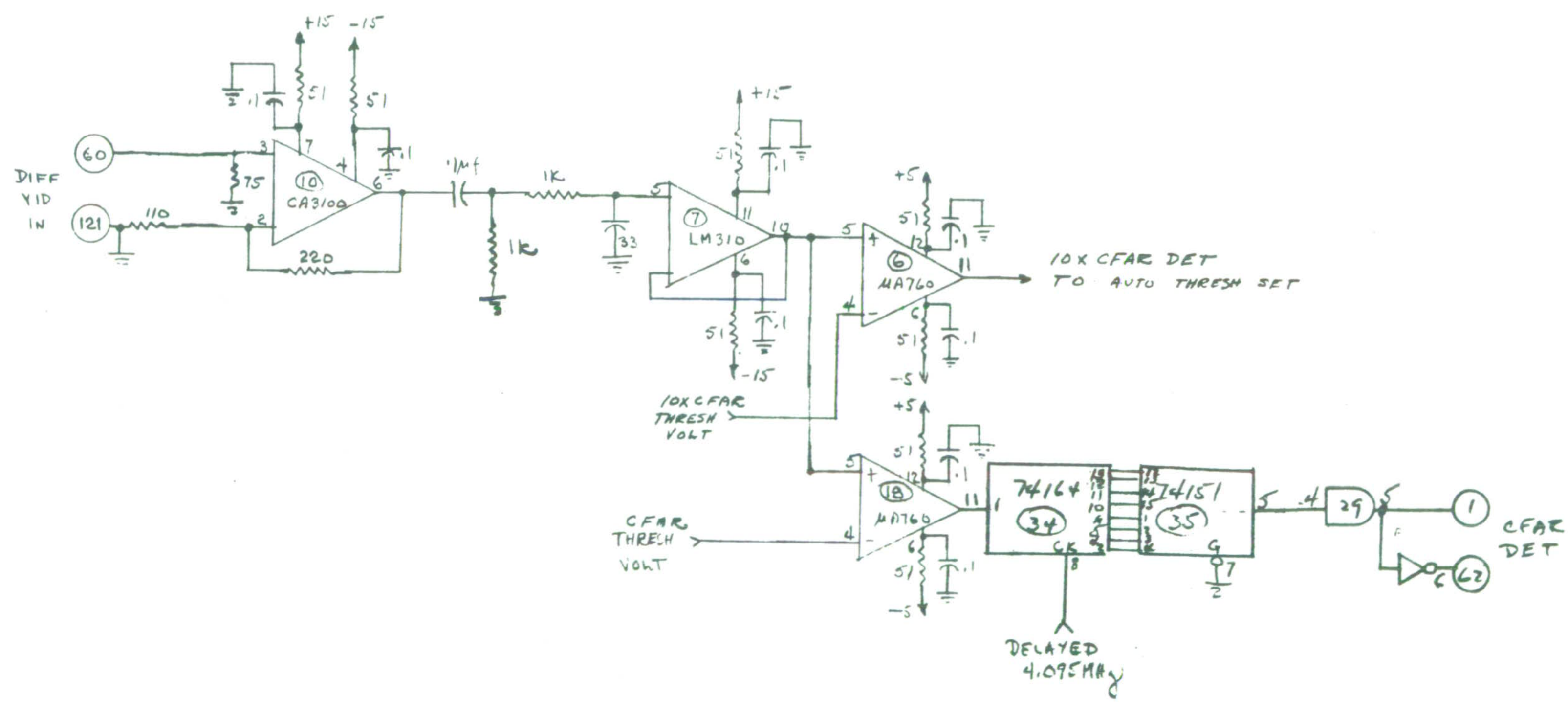


Fig. AI-2. CFAR Detector Circuits (Sheet 2 of 5) CFAR Video Processor.

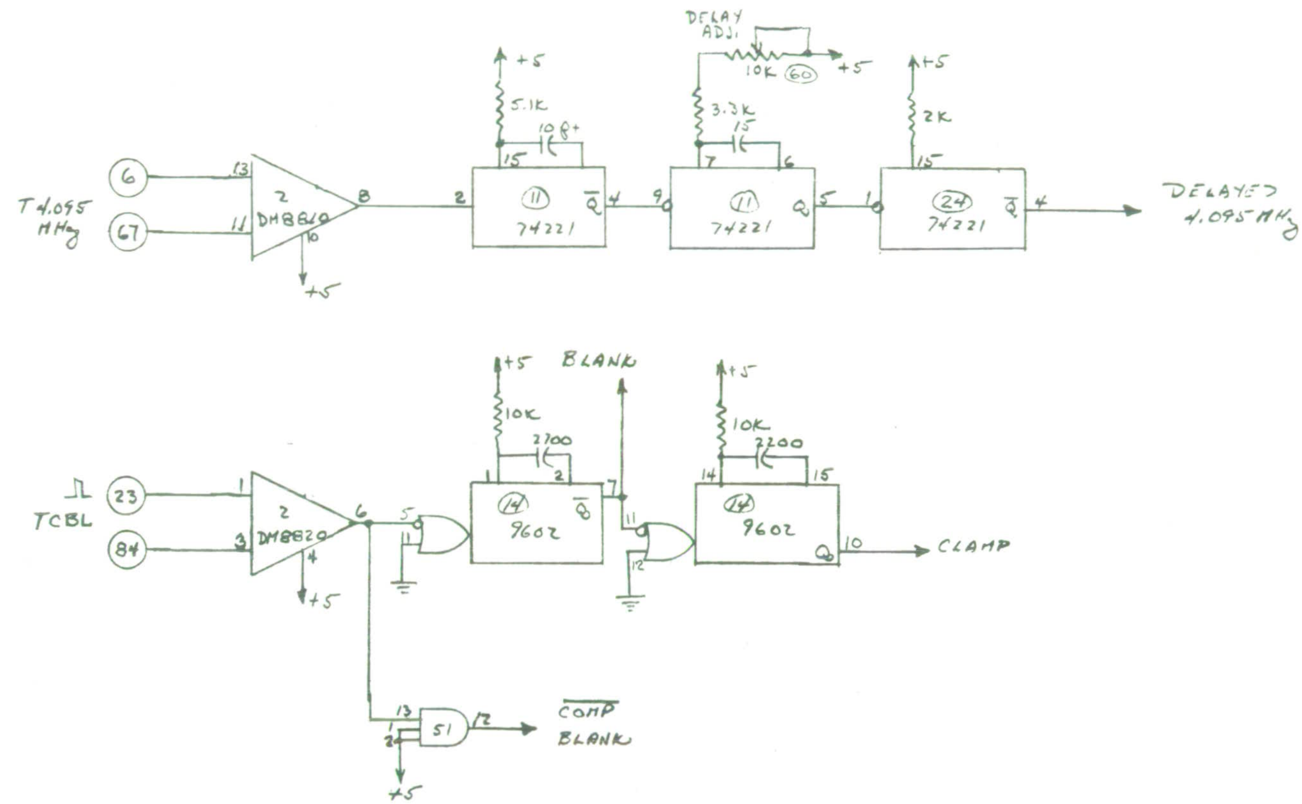


Fig. AI-3. CFAR Timing Circuits (Sheet 3 of 5) CFAR Video Processor.

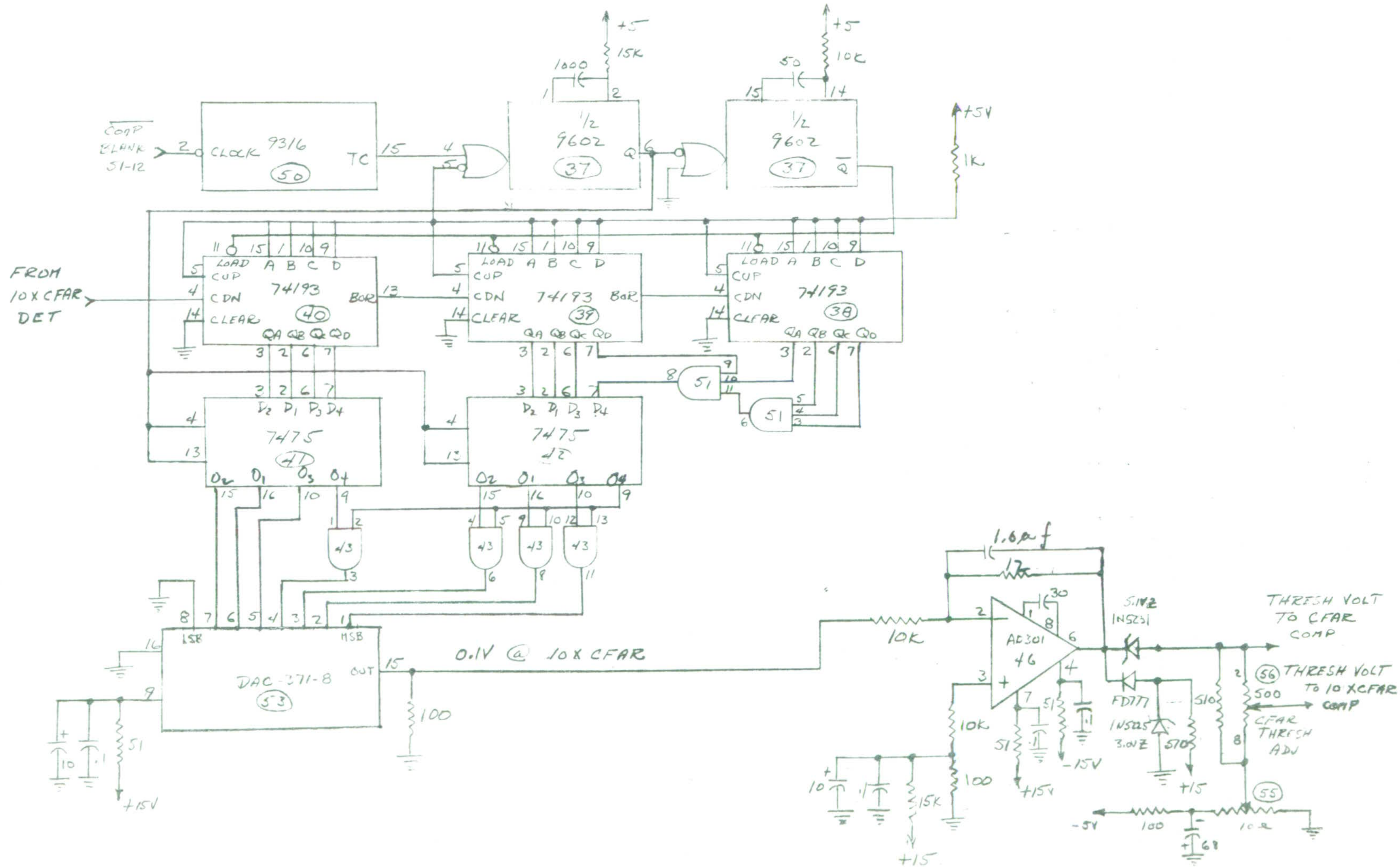


Fig. AI-4. Automatic Threshold Set (Sheet 4 of 5) CFAR Video Processor.

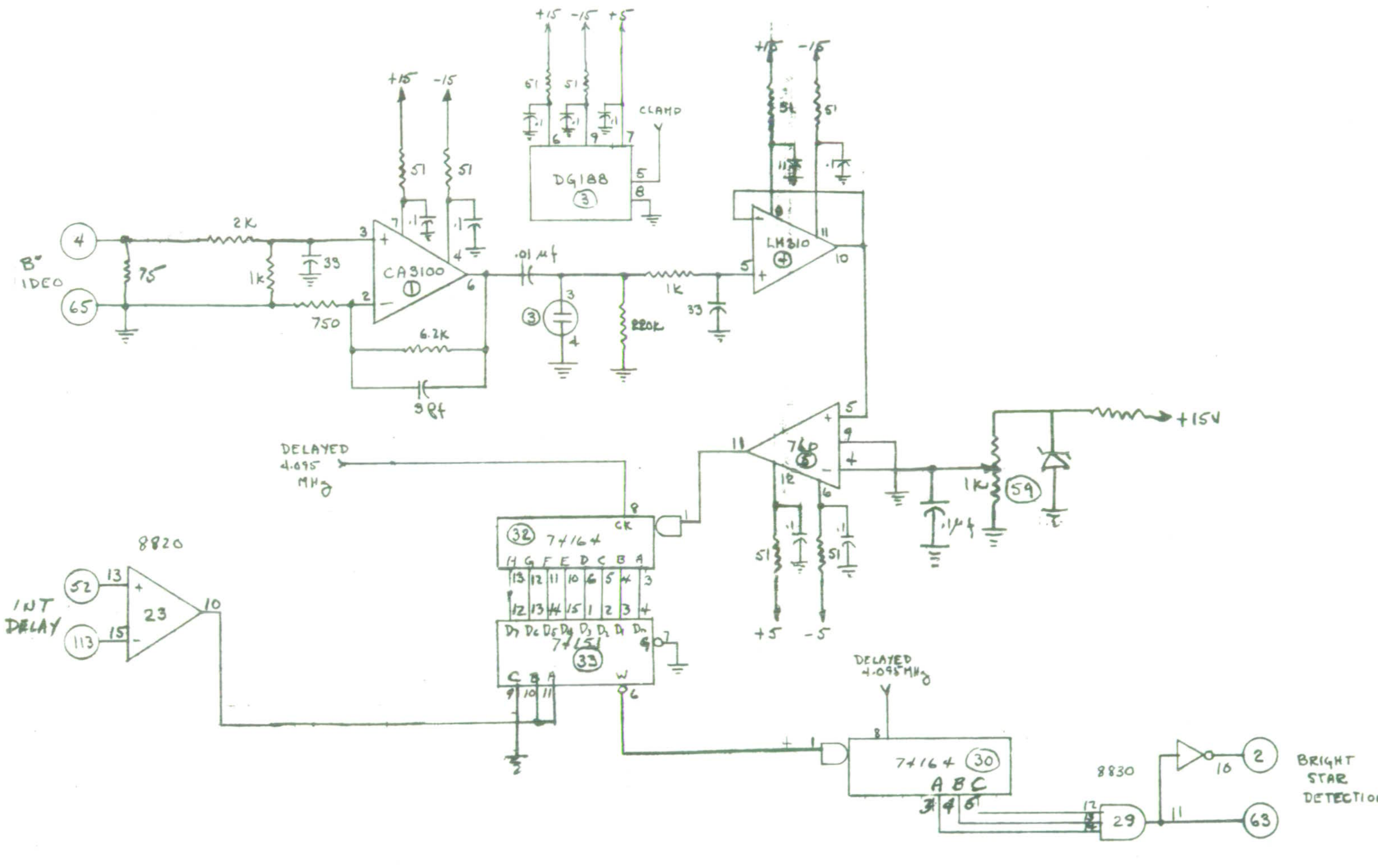


Fig. AI-5. CFAR Video Processor Bright Star Detector (Sheet 5 of 5).

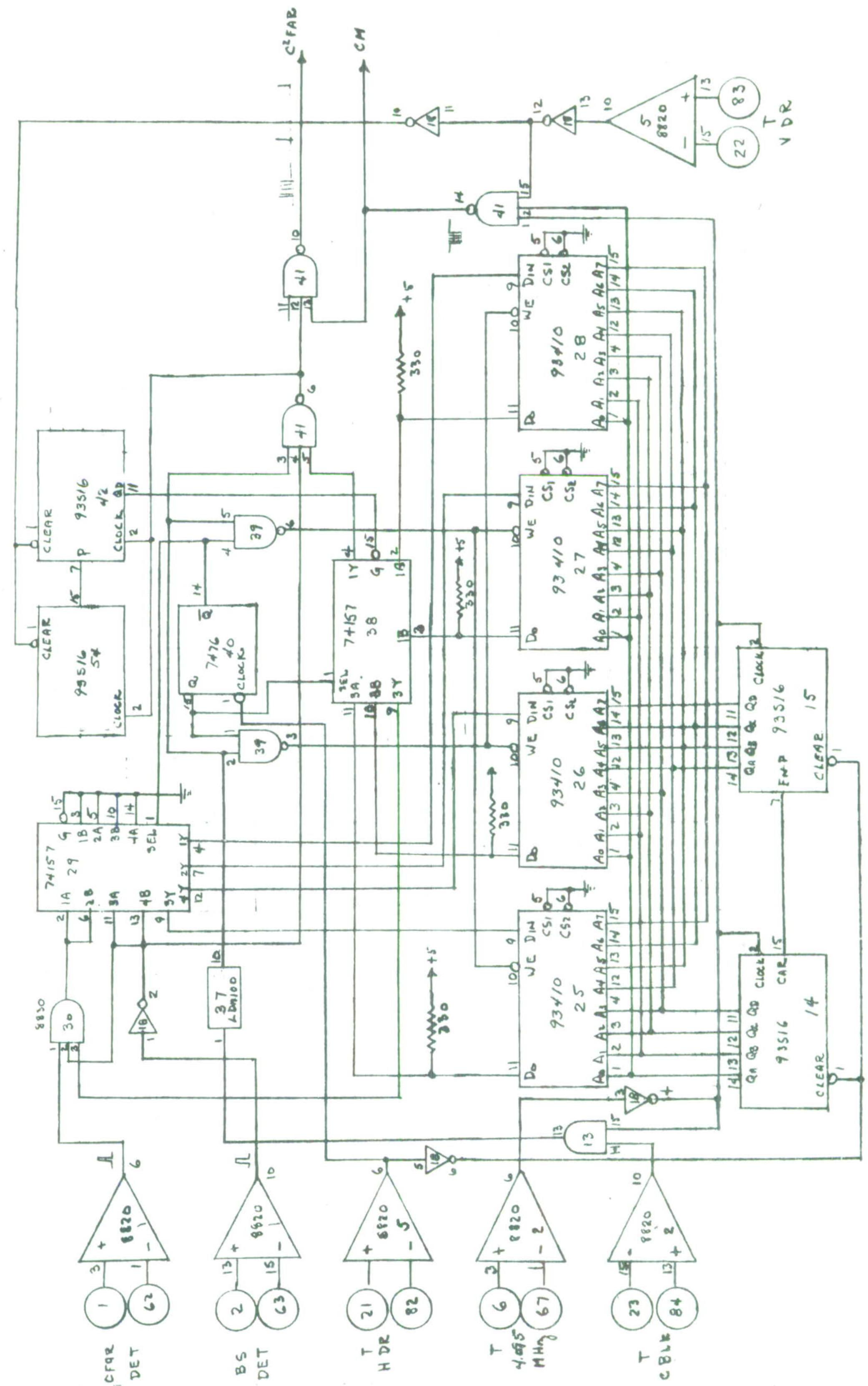


Fig. A1-6. Correlator Control Board Bright Star Blanking (Sheet 1 of 3).

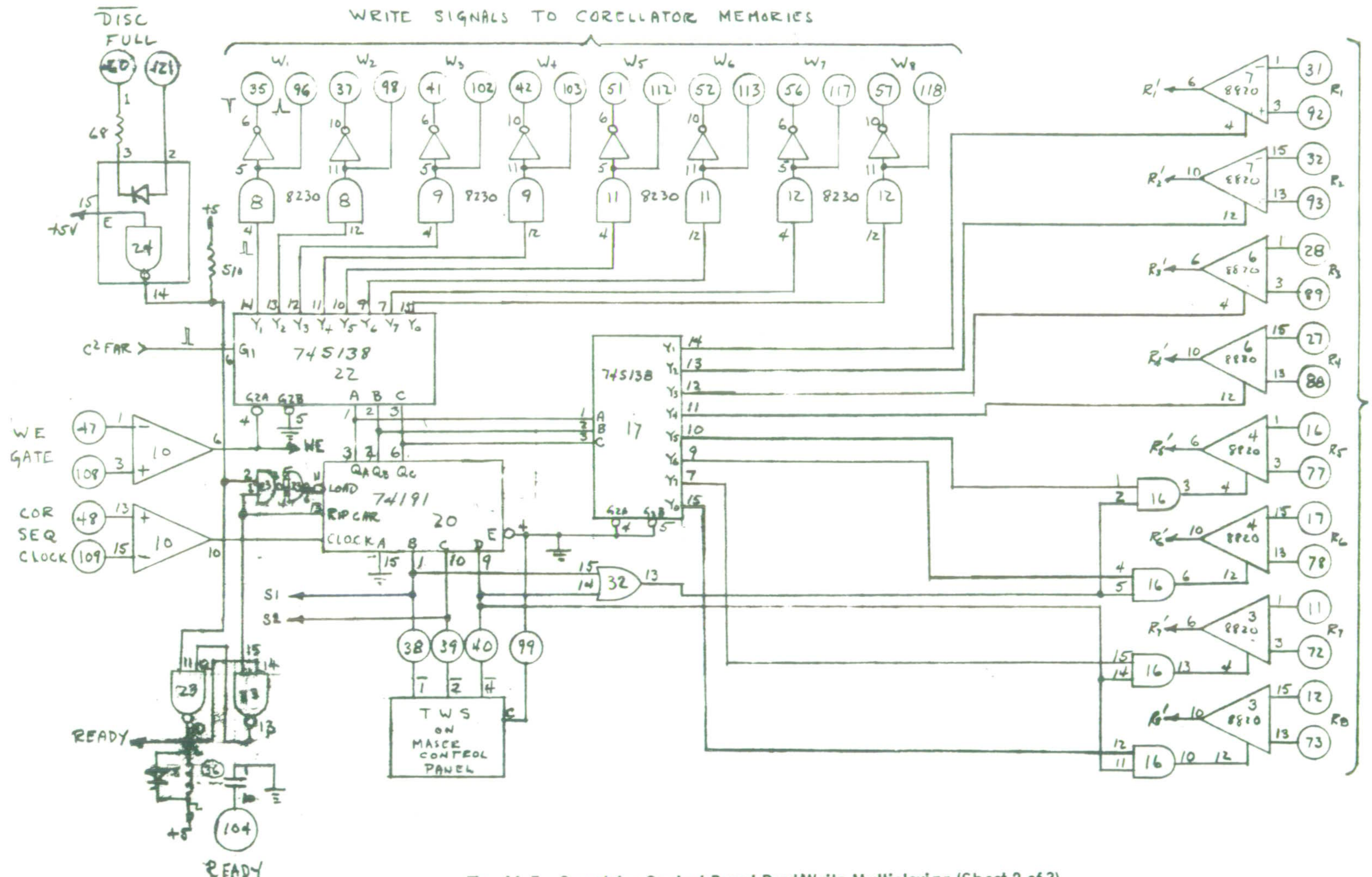


Fig. AI-7. Correlator Control Board Read/Write Multiplexing (Sheet 2 of 3).

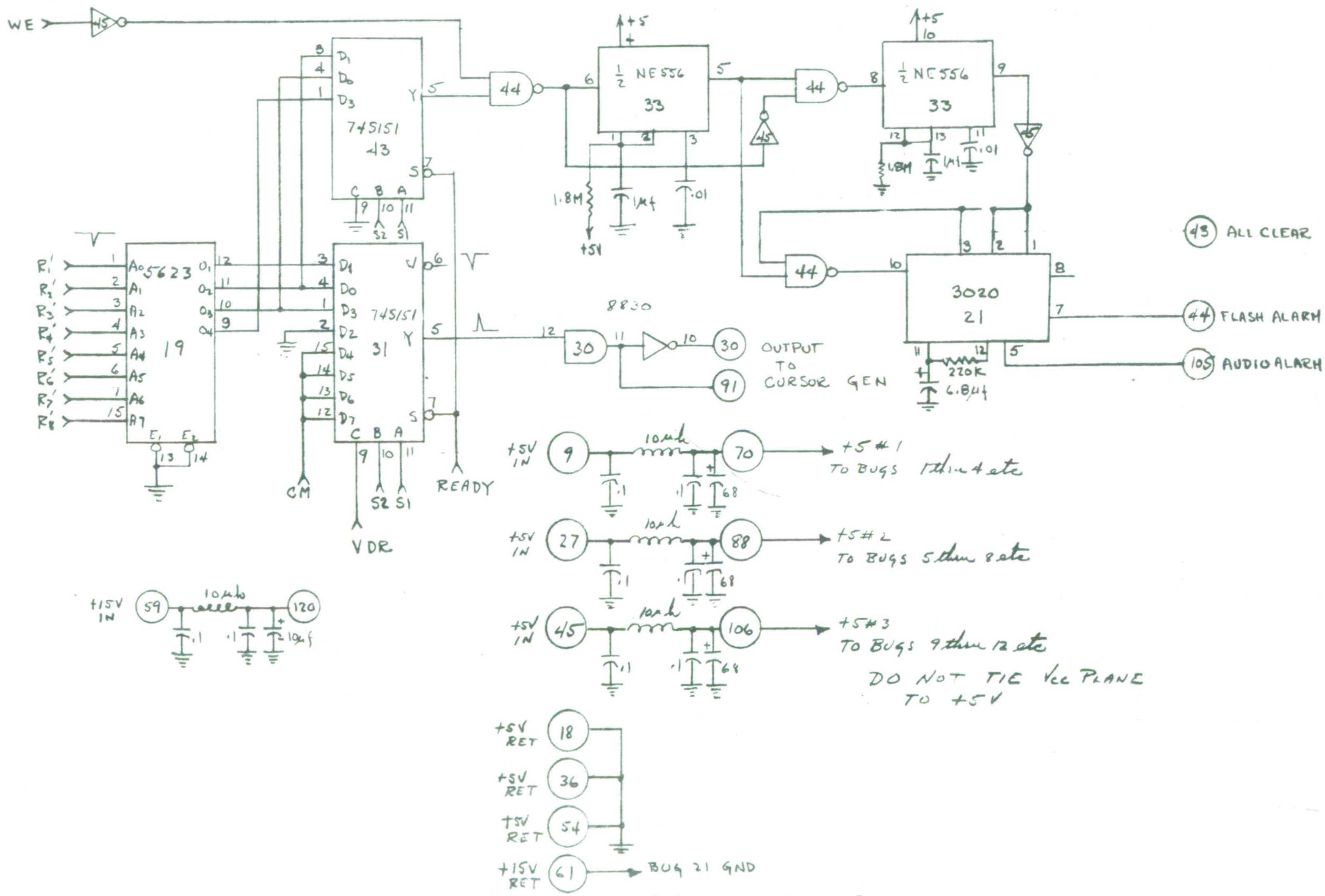


Fig. AI-8. Correlator Control Board Correlator (Sheet 3 of 3).

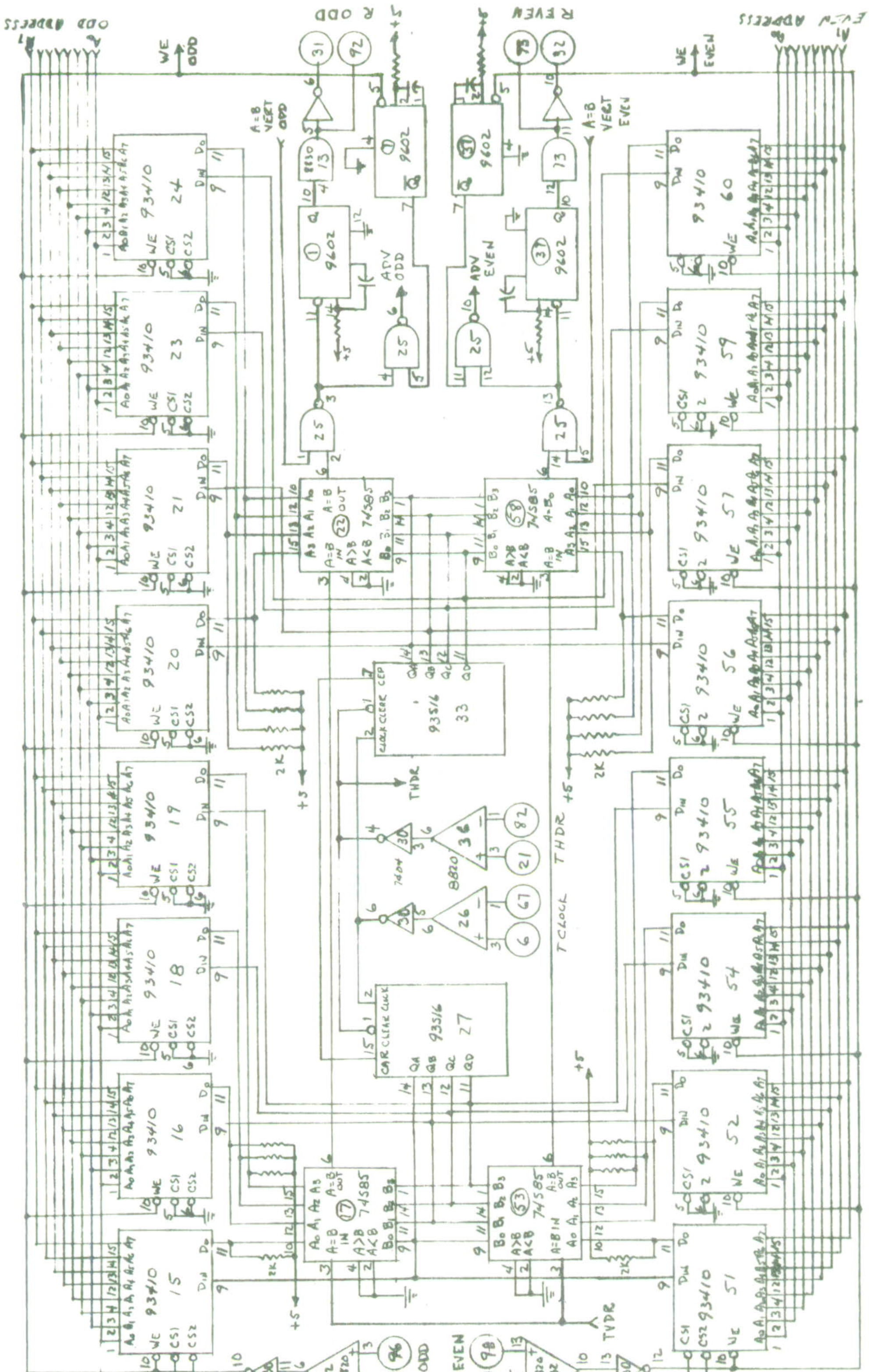


Fig. AI-9. Corellator Memory - Horizontal (Sheet 1 of 2).

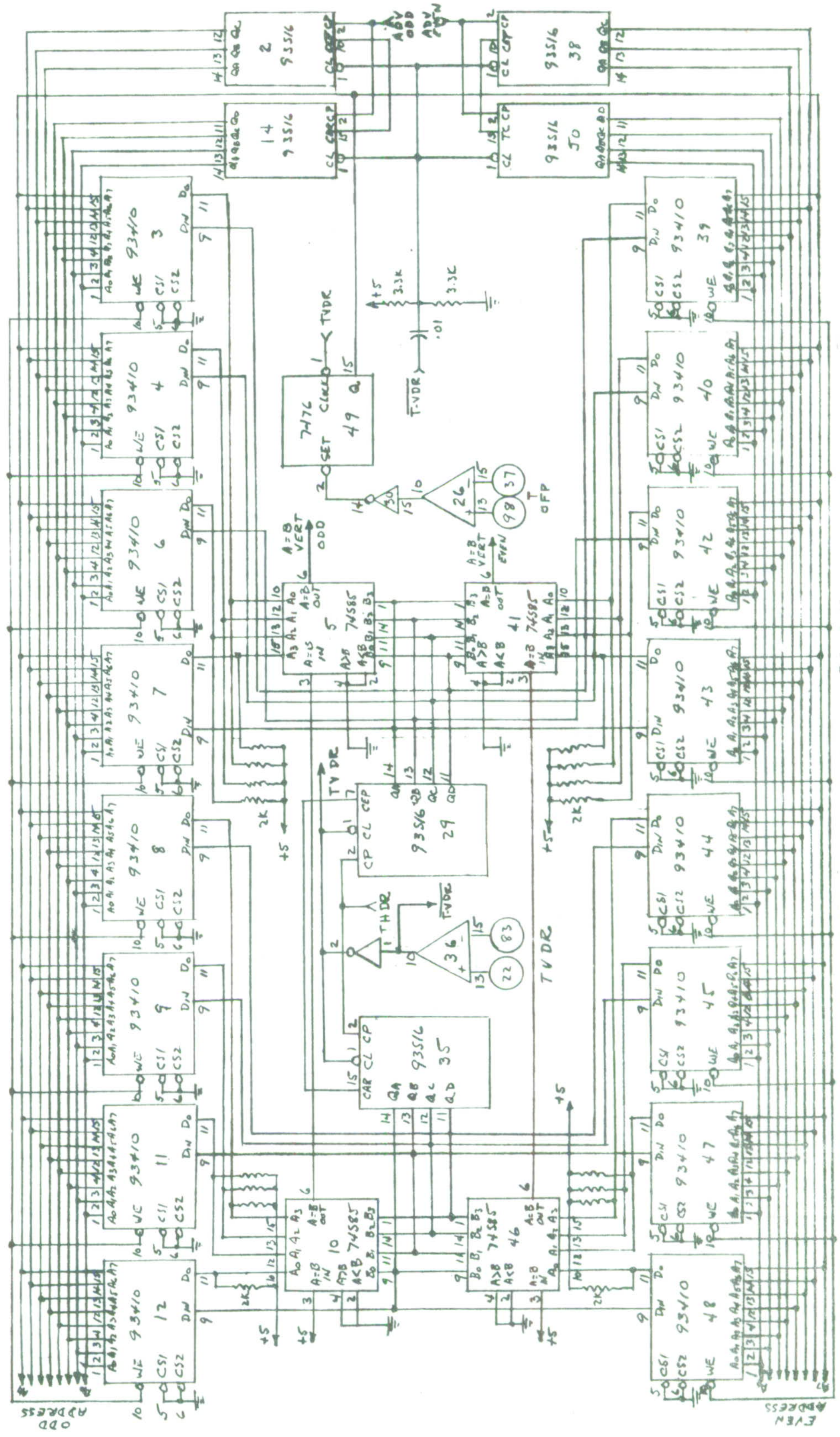


Fig. AI-10. Correlator Memory – Vertical (Sheet 2 of 2).

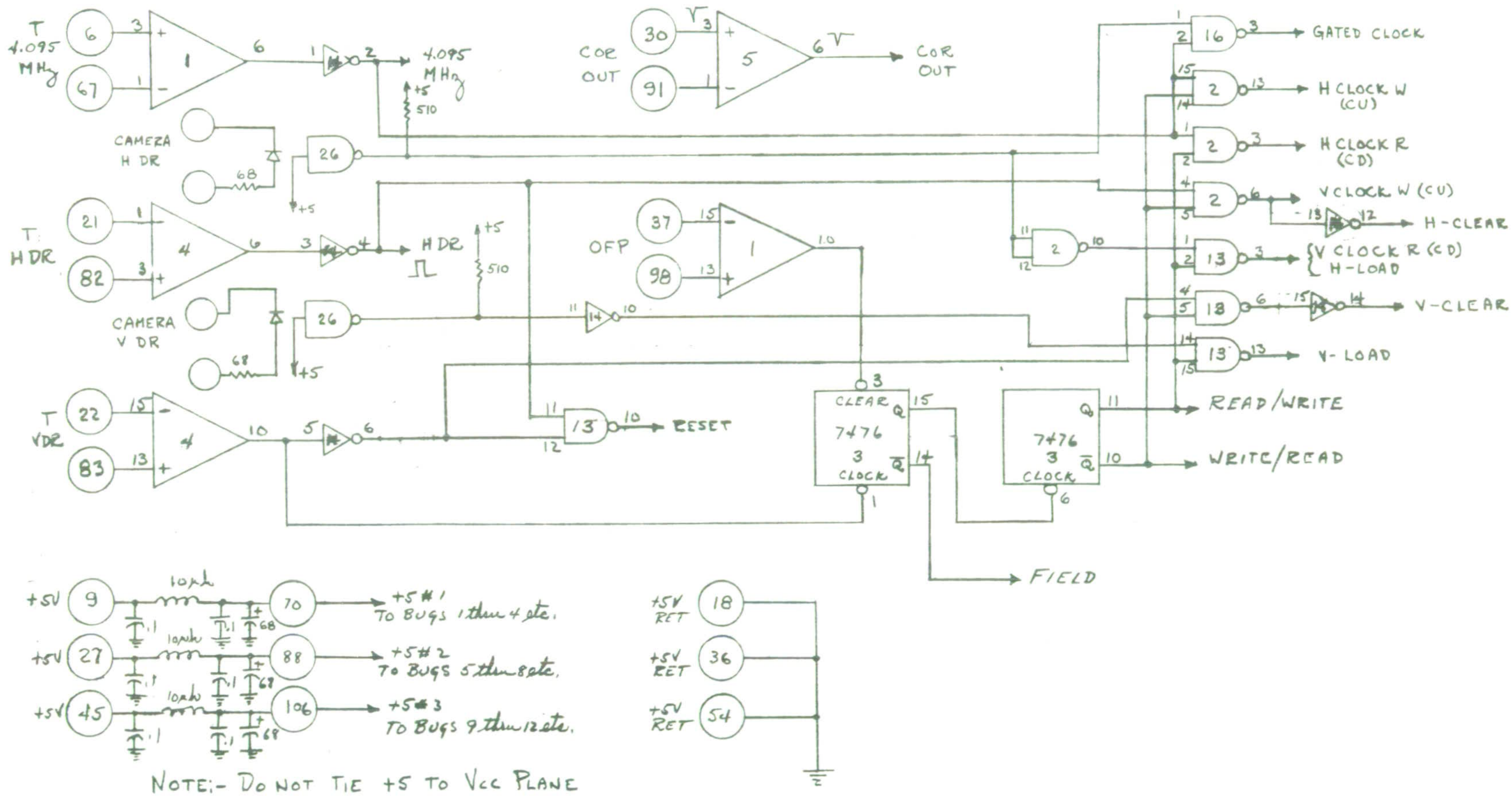


Fig. AI-11. Cursor Gen Interface Logic (Sheet 1 of 3).

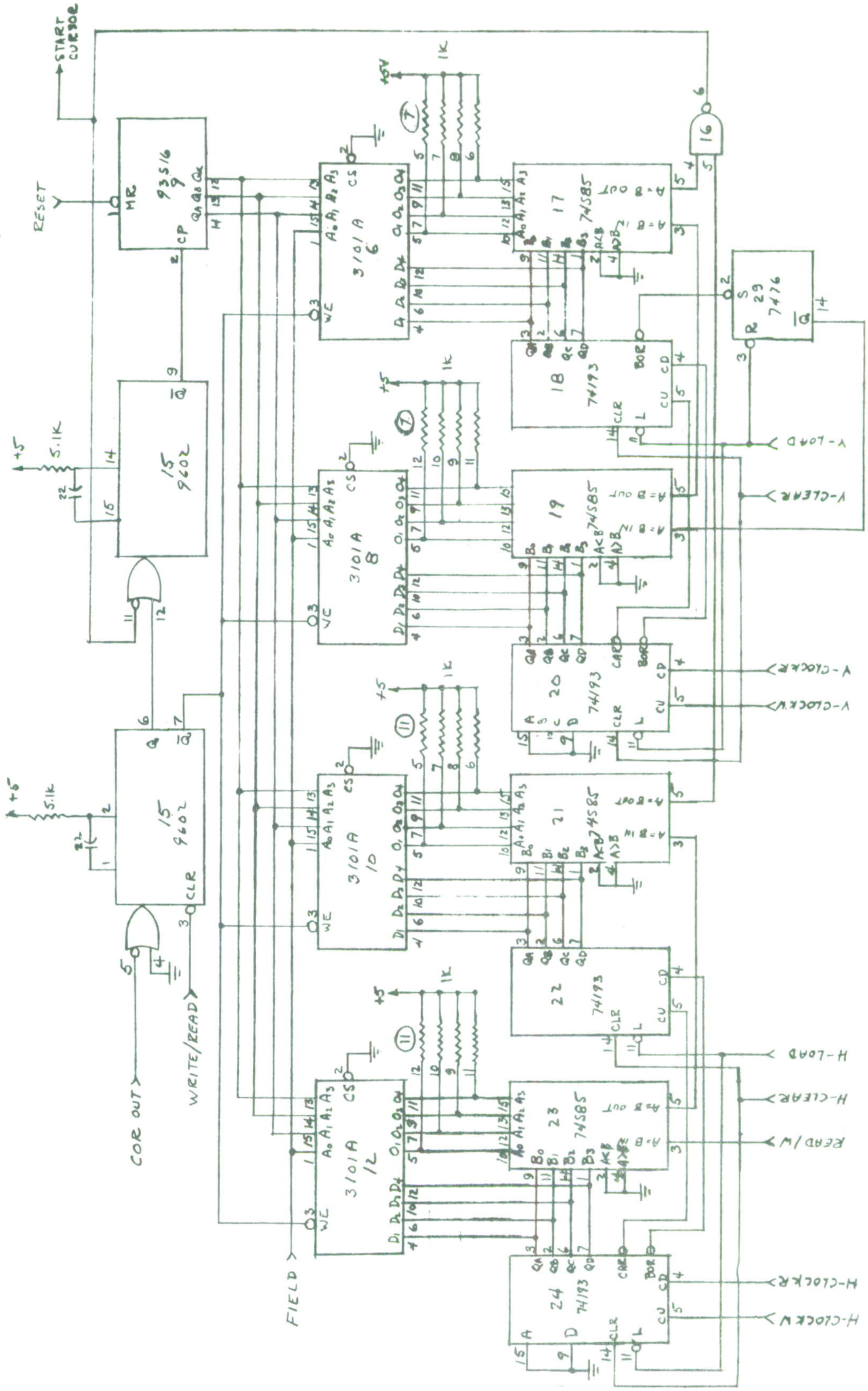


Fig. AI-12. Cursor Gen Buffer Memory (Sheet 2 of 3).

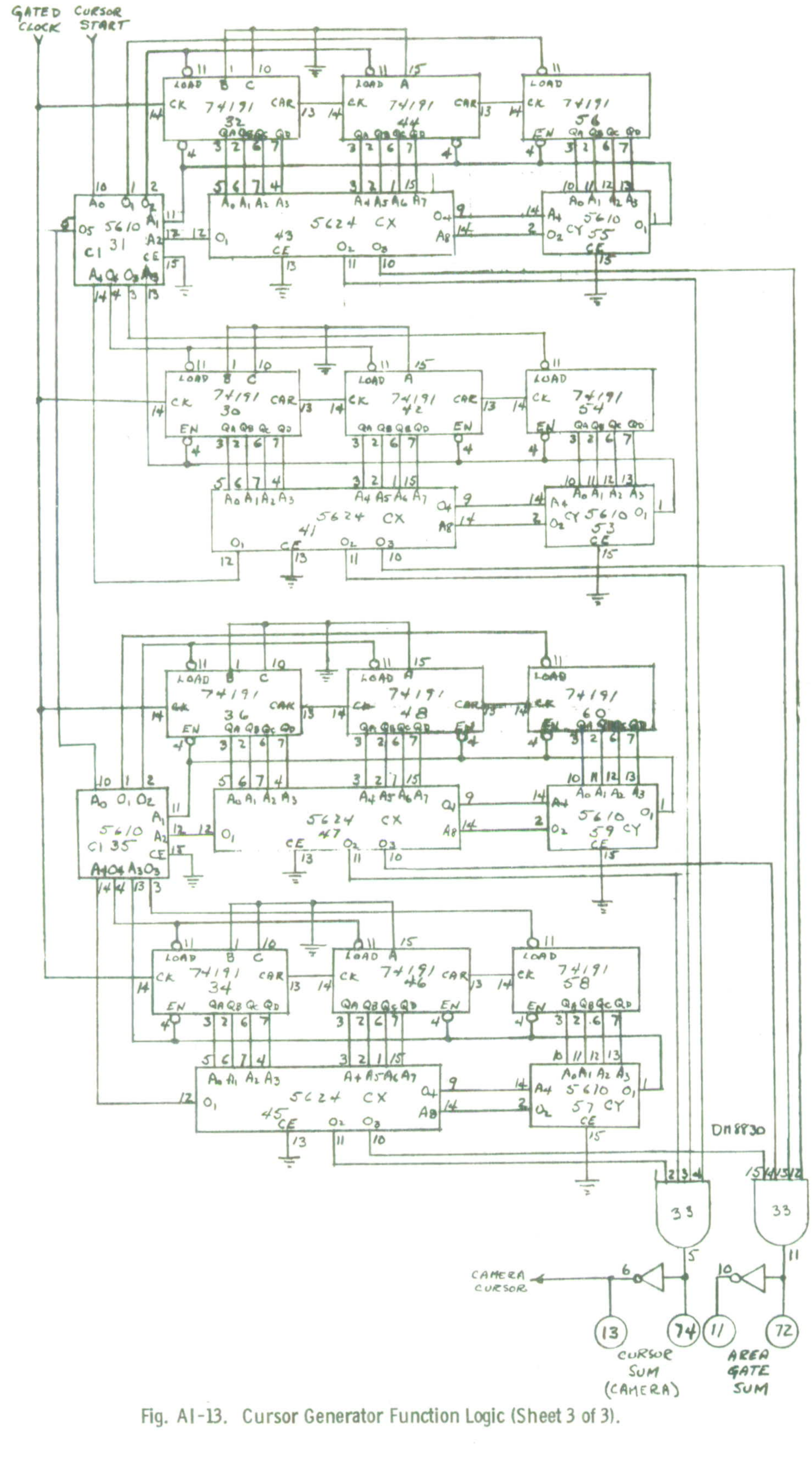


Fig. A1-13. Cursor Generator Function Logic (Sheet 3 of 3).

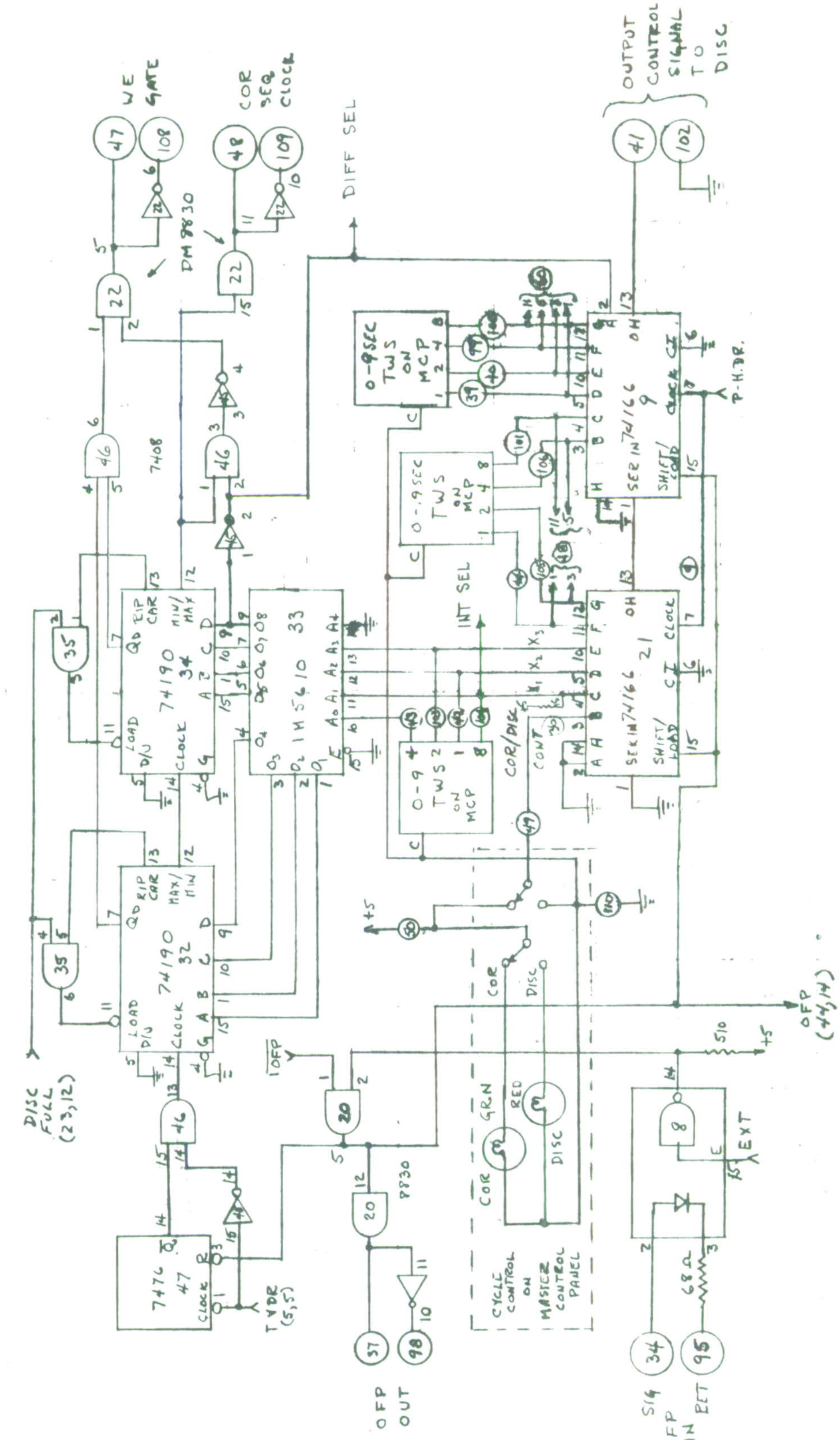


Fig. AI-14. Interface Logic Cycling Control Encoder (Sheet 1 of 6).

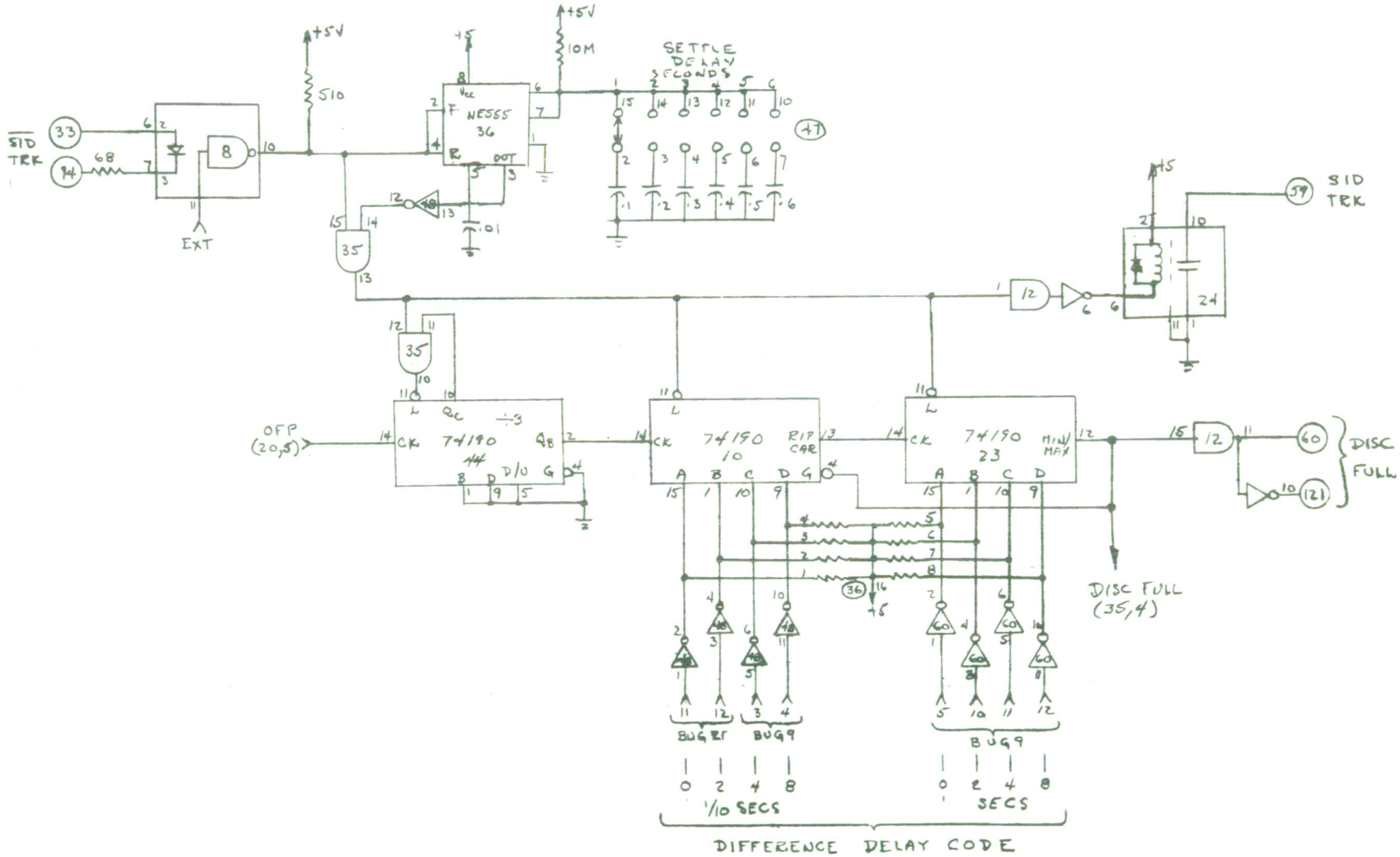


Fig. AI-15. Interface Logic Pipeline Delay Timing (Sheet 2 of 6).

	$\overline{4}$ A_0	$\overline{8}$ A_1	$\overline{1}$ A_2	$\overline{2}$ A_3	A_4	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
10	1	0	0	1	0	0	0	0	1	1	0	1	0
14	1	0	1	1	0	0	0	0	1	1	0	0	0
3	0	1	0	0	0	0	1	1	0	1	0	1	0
7	0	1	1	0	0	1	1	0	0	1	0	1	0
11	0	1	0	1	0	1	1	0	0	1	1	0	0
15	0	1	1	1	0	1	1	0	0	1	0	0	0
	1	1	0	0	0	0	0	0	1	0	0	0	1
	1	1	1	0	0	0	0	0	1	0	0	0	1
	1	1	0	1	0	0	0	0	1	0	0	0	1
	1	1	1	1	0	0	0	0	1	0	0	0	1

Fig. AI-16. Interface Logic Cycling Control Encoder IM 5610 is Programming (Sheet 3 of 6).

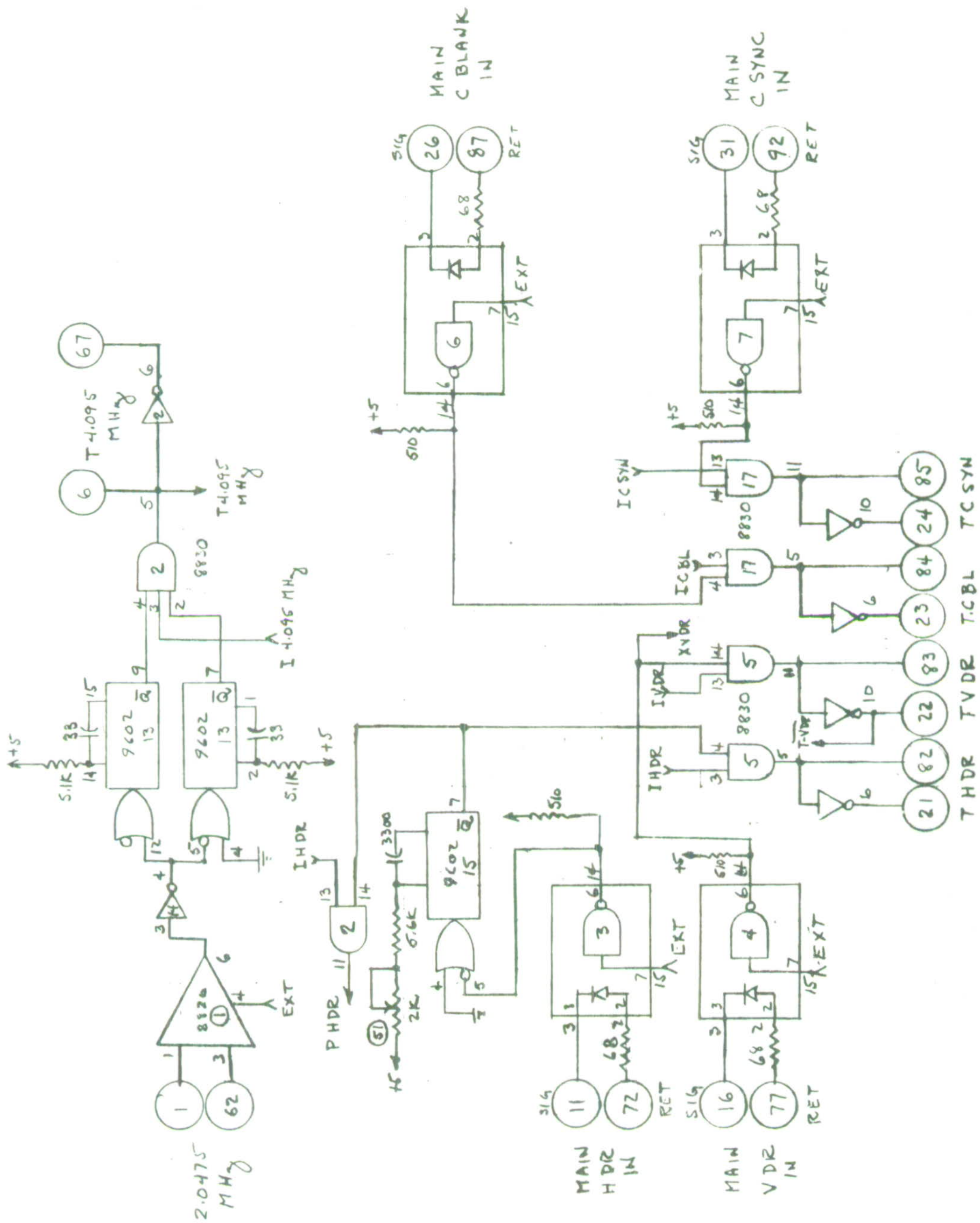


Fig. AI-17. Interface Logic Main/Mon Sync & Video Sw (Sheet 4 of 6).

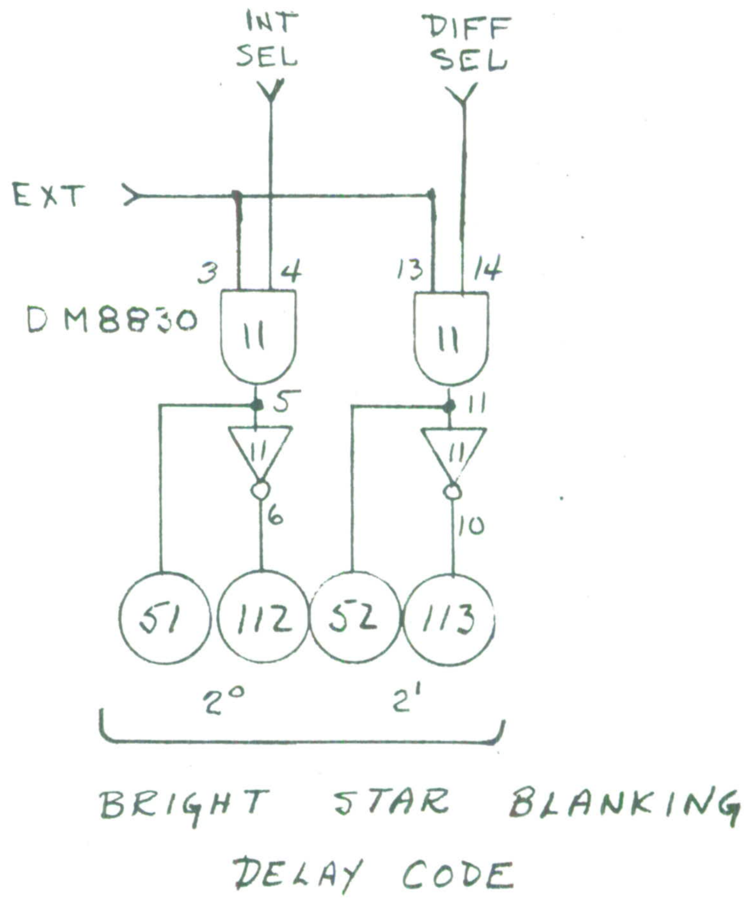


Fig. AI-18. Interface logic delay equalizer. Sheet 5 of 6.

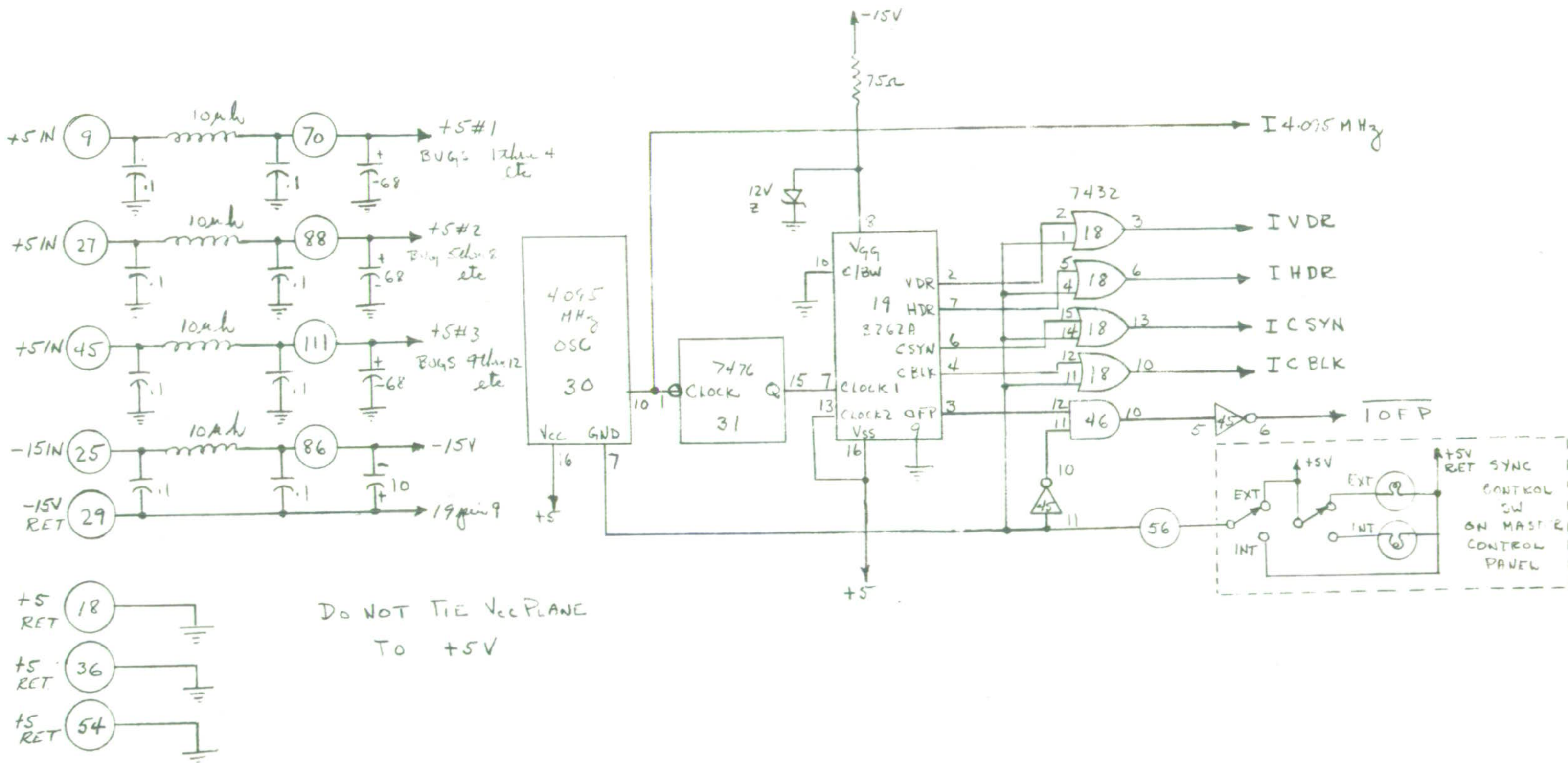


Fig. AI-19. Interface Logic Internal Sync Gen (Sheet 6 of 6).

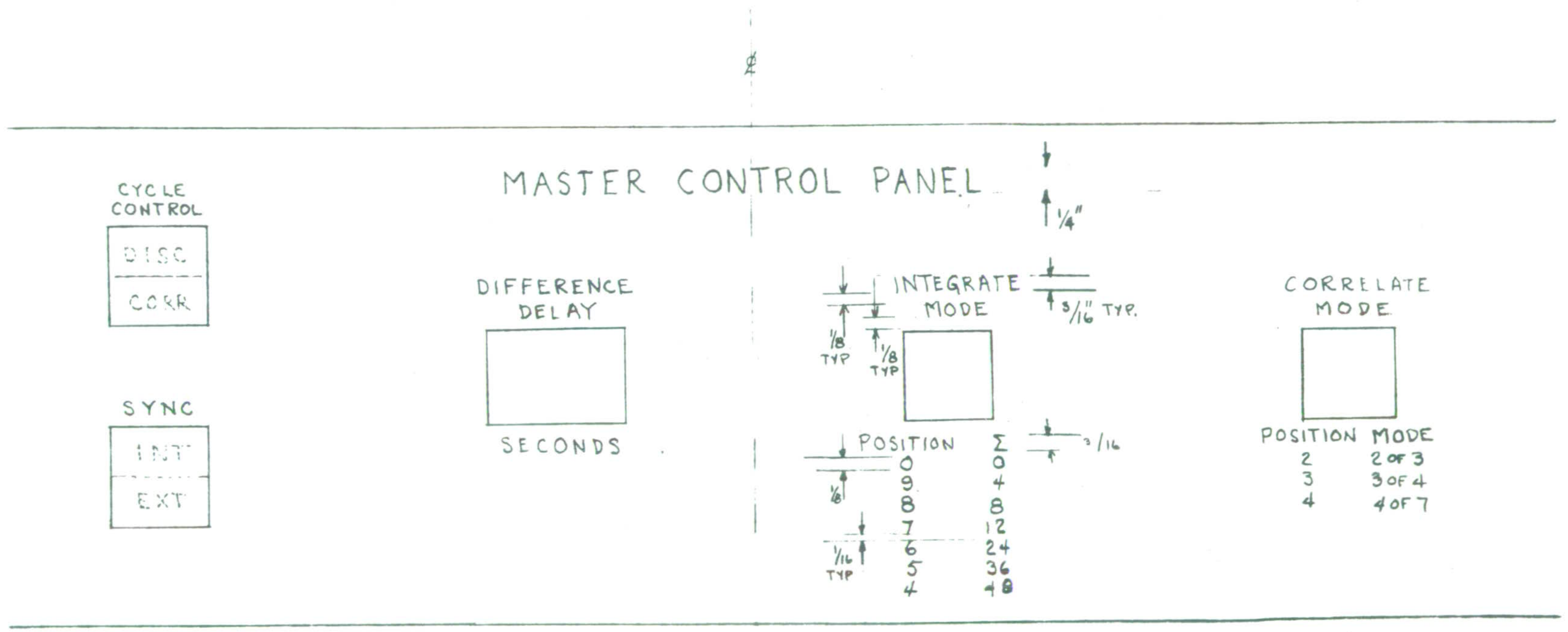


Fig. AI-20. Master Control Panel Engraving – White Fill.

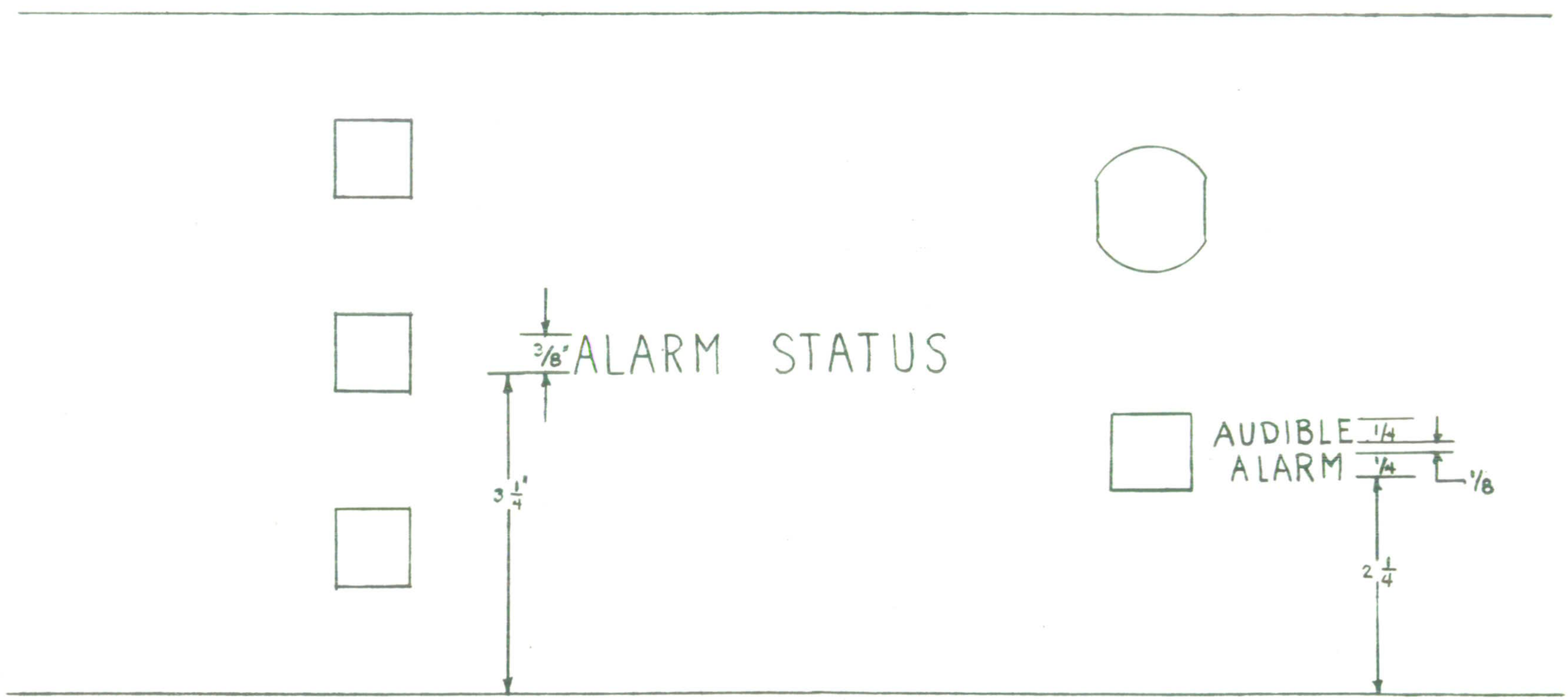


Fig. AI-21. Alarm Status Panel Engraving Black Anodize After Machining – White Fill on Engraving (Sheet 2 of 2).

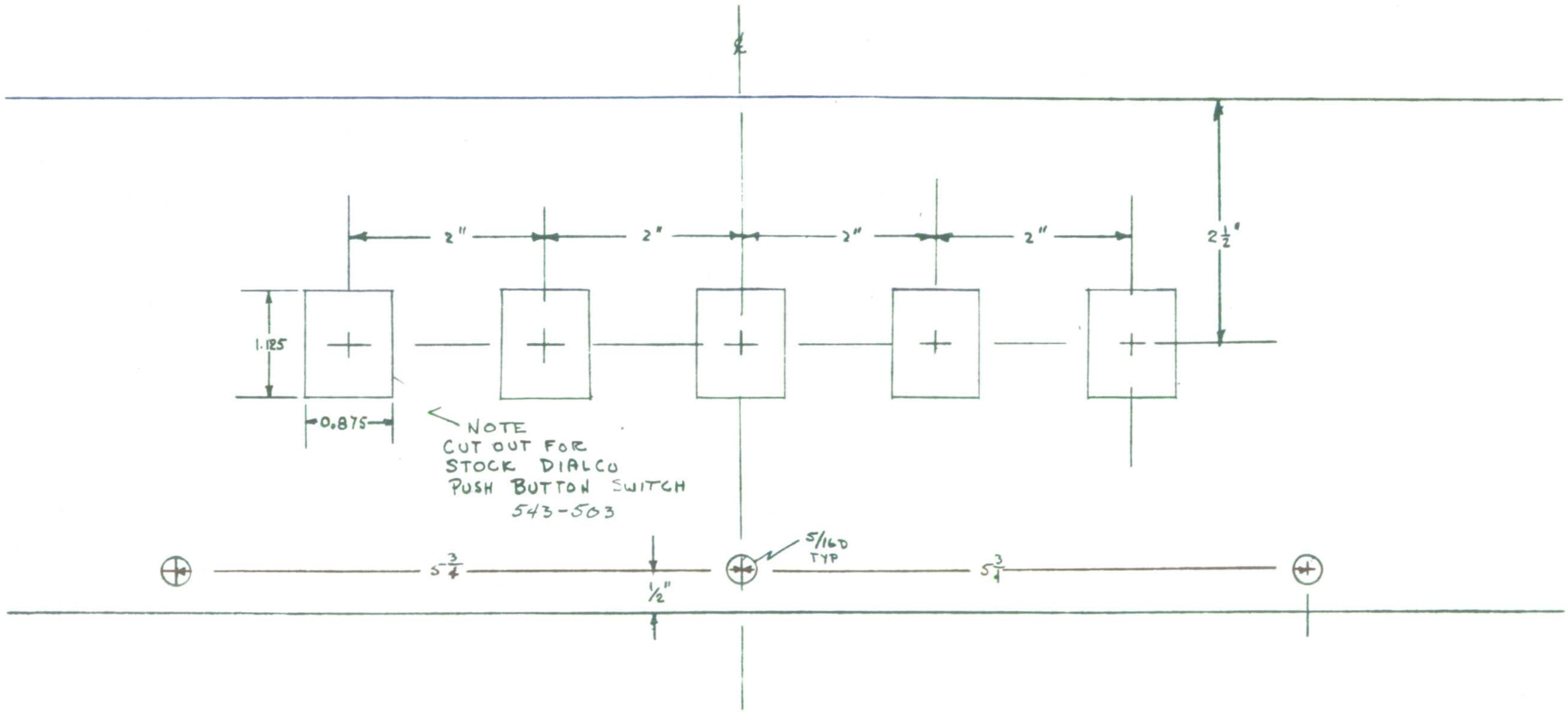


Fig. AI-22. Power Supply Control & Status Hole Cutouts. Use Standard 5-1/4" 19" 1/8" Unpainted Aluminum Panel (Sheet 1 of 2).

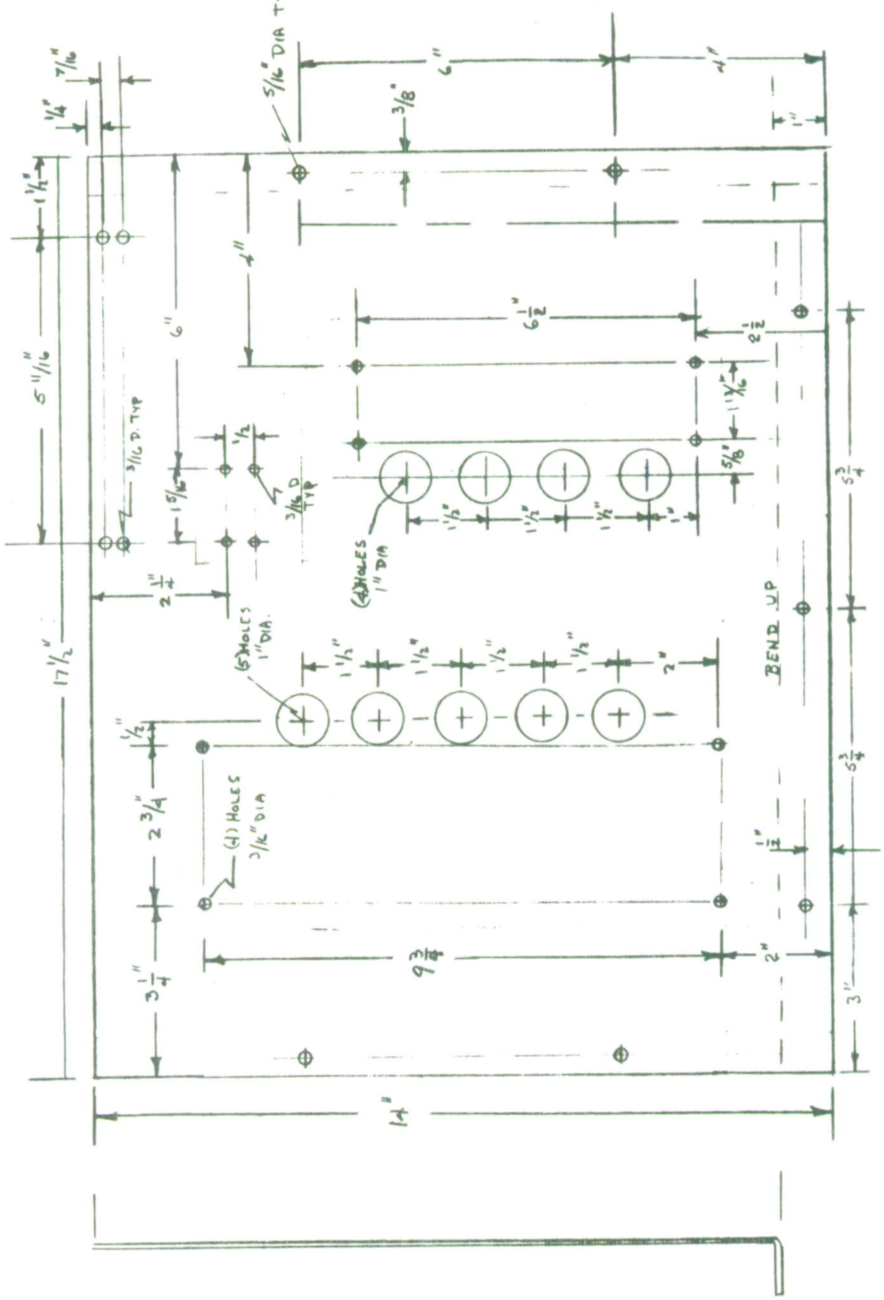


Fig. A1-23. Power Supply Mounting Plate.

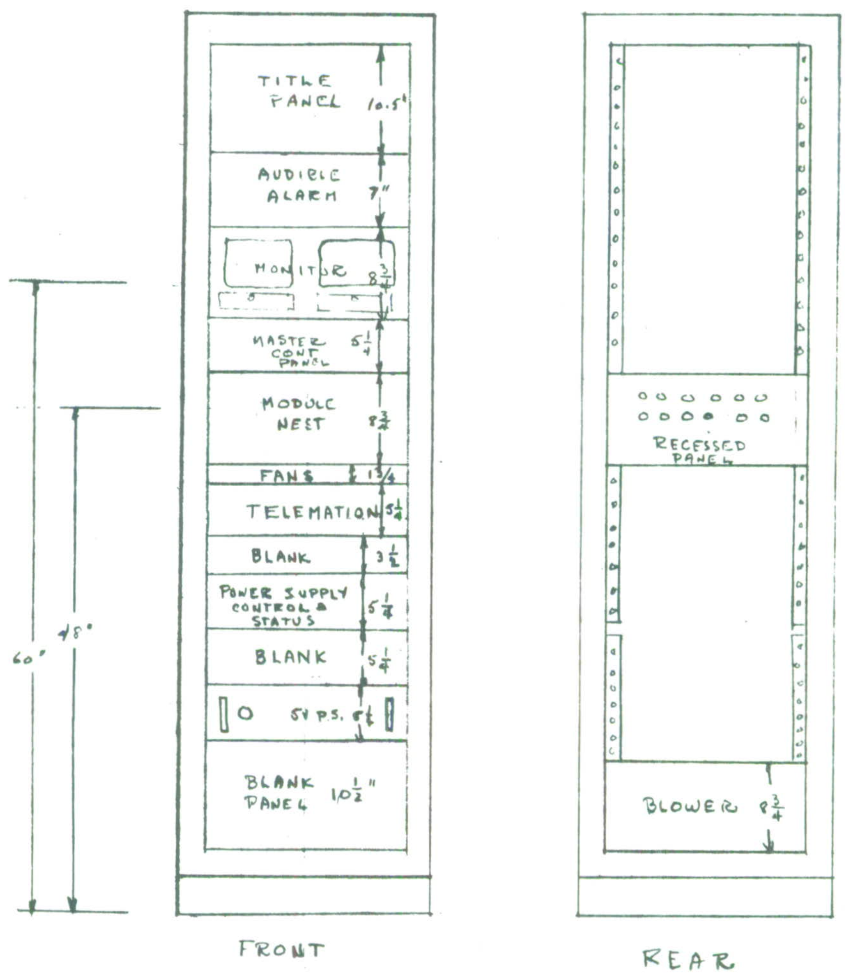


Fig. AI-24. CFAR Detector & Correlator Panel Arrangement (Sheet 1 of 1).

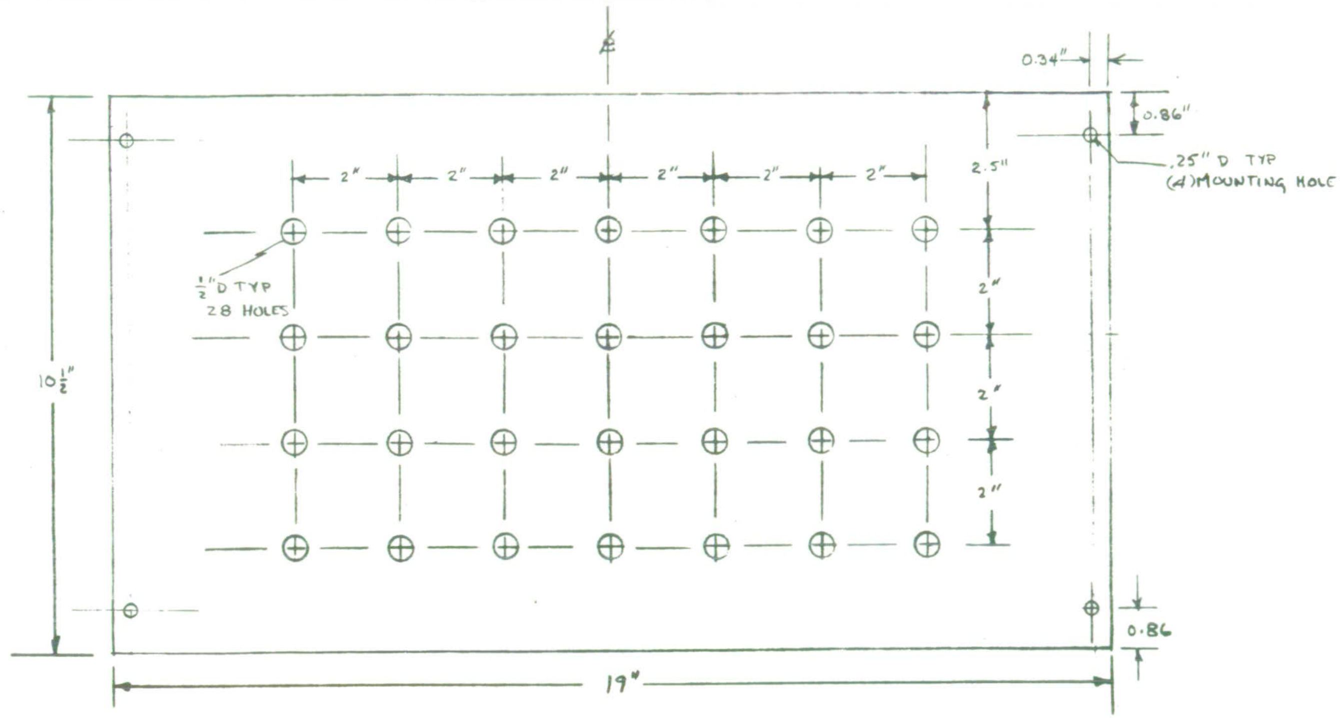


Fig. A1-25. Interface Panel Hole Pattern Cut From 3/16" Black Phenolic (Sheet 1 of 2).

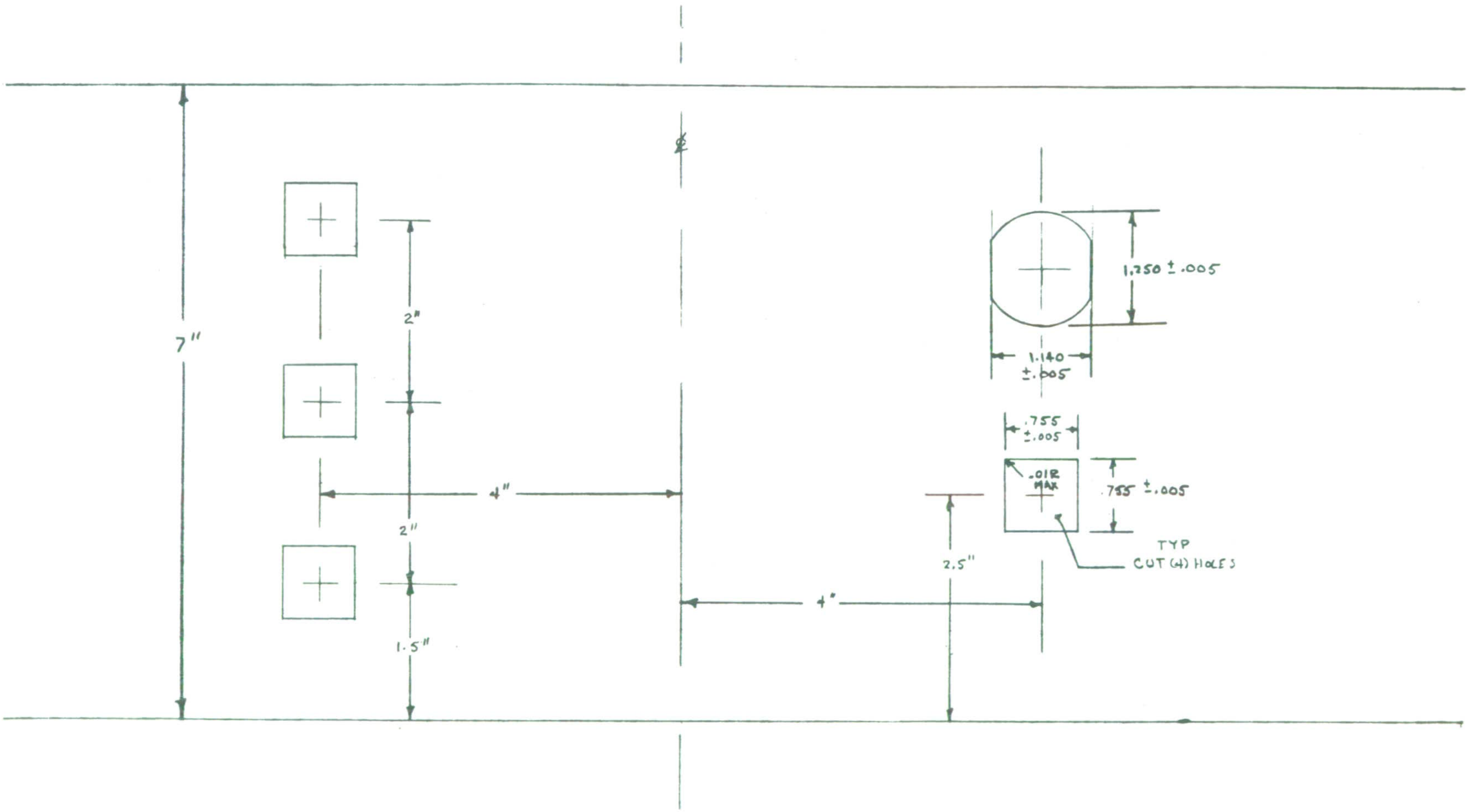


Fig. AI-26. Alarm Status Panel Hole Cutouts Standard 19" 7" 1/8" Bare Aluminum Panel (Sheet 1 of 2).

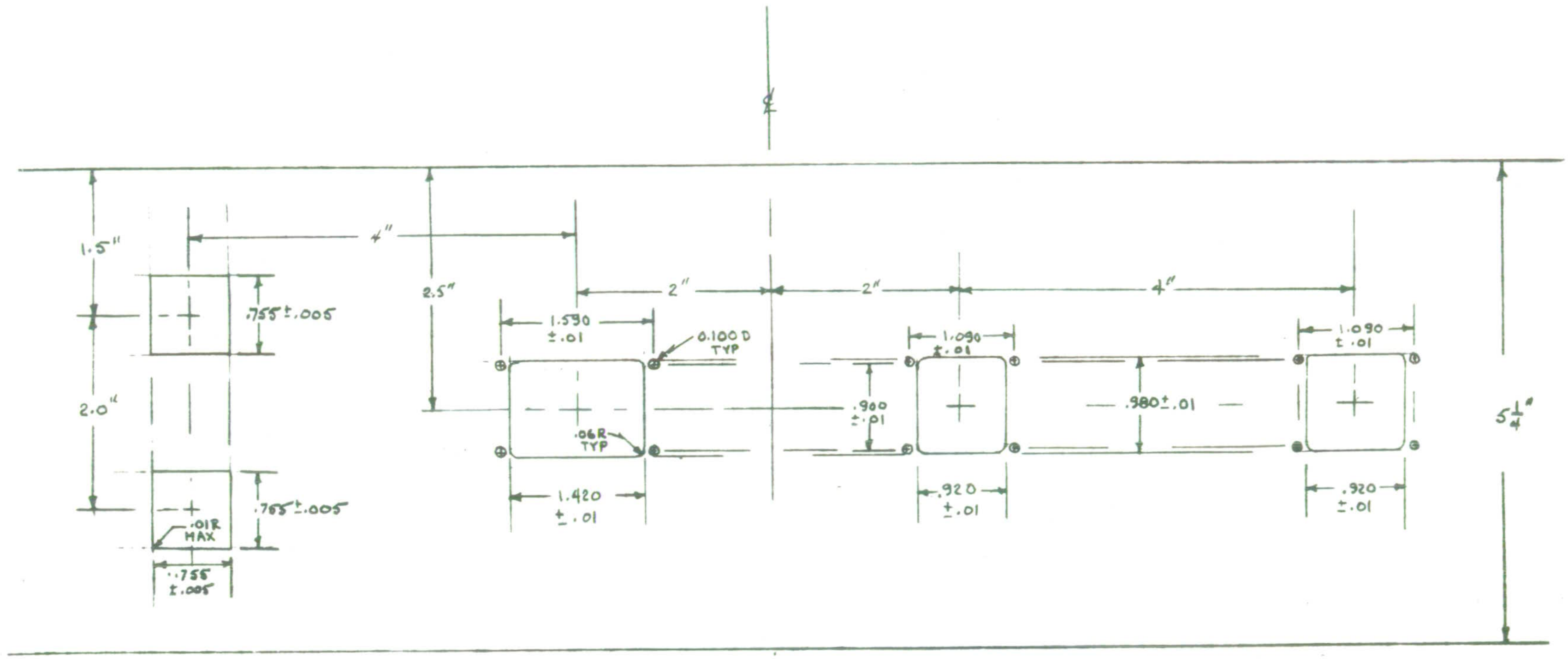


Fig. A1-27. Master Control Panel Hole Cutouts.

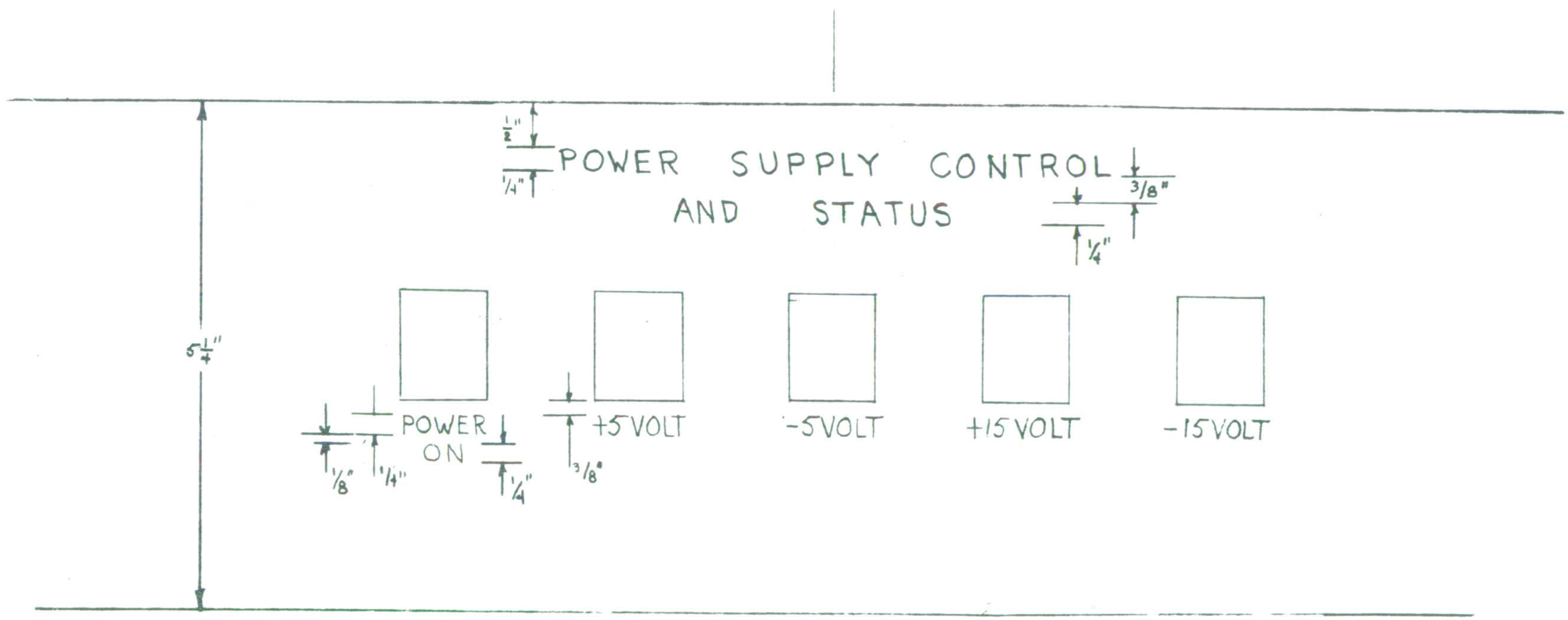


Fig. A1-28. Power Supply Contol & Status Front Panel Engraving Black Anodize After Machining White Fill on Engraving (Sheet 2 of 2).

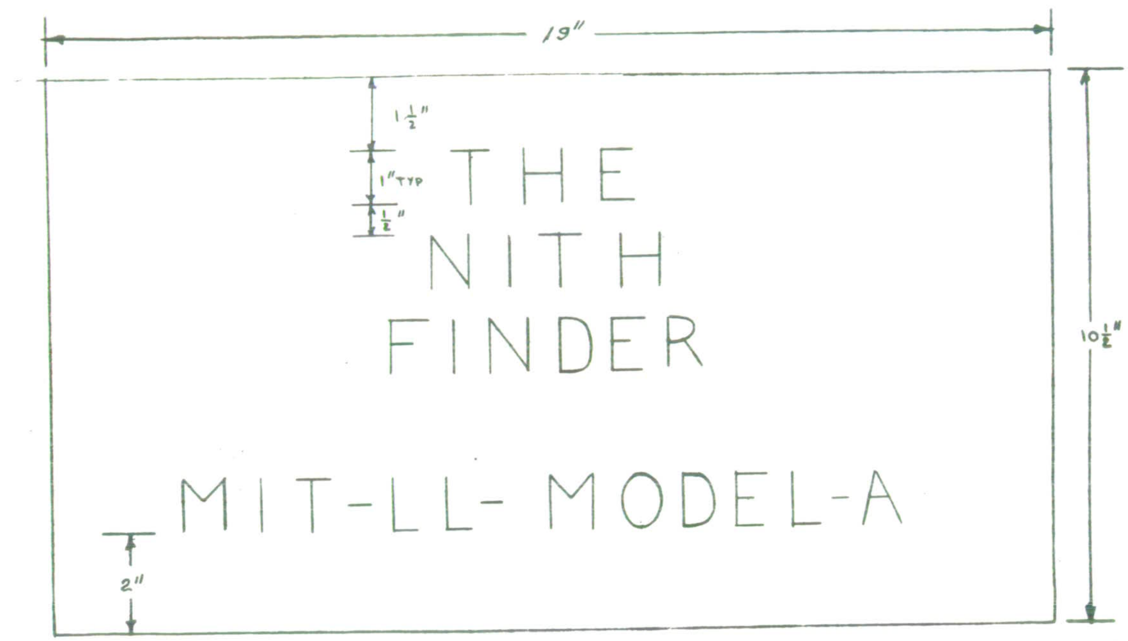


Fig. AI-29. Title Panel Standard 10-1/2" 19" 1/8" Aluminum Panel Black Anodize Engrave & White Fill

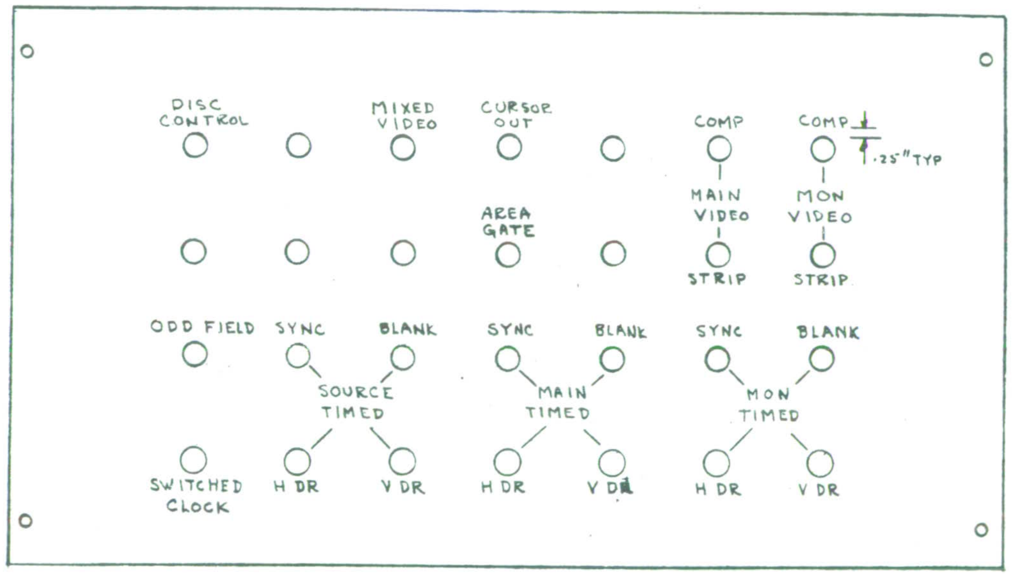


Fig. AI-30. Interface Panel Engraving All Lettering 3/16" High – White Fill (Sheet 2 of 2).

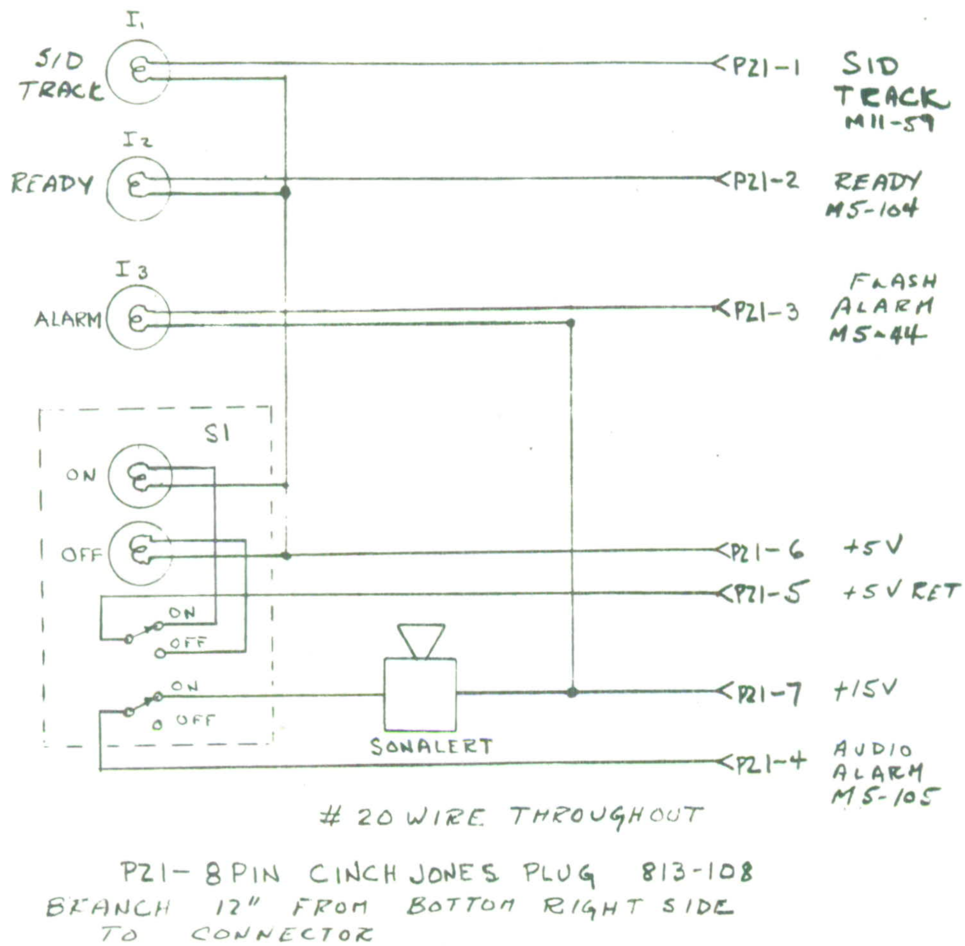


Fig. AI-31. Alarm status panel wiring sheet 1 of 1.

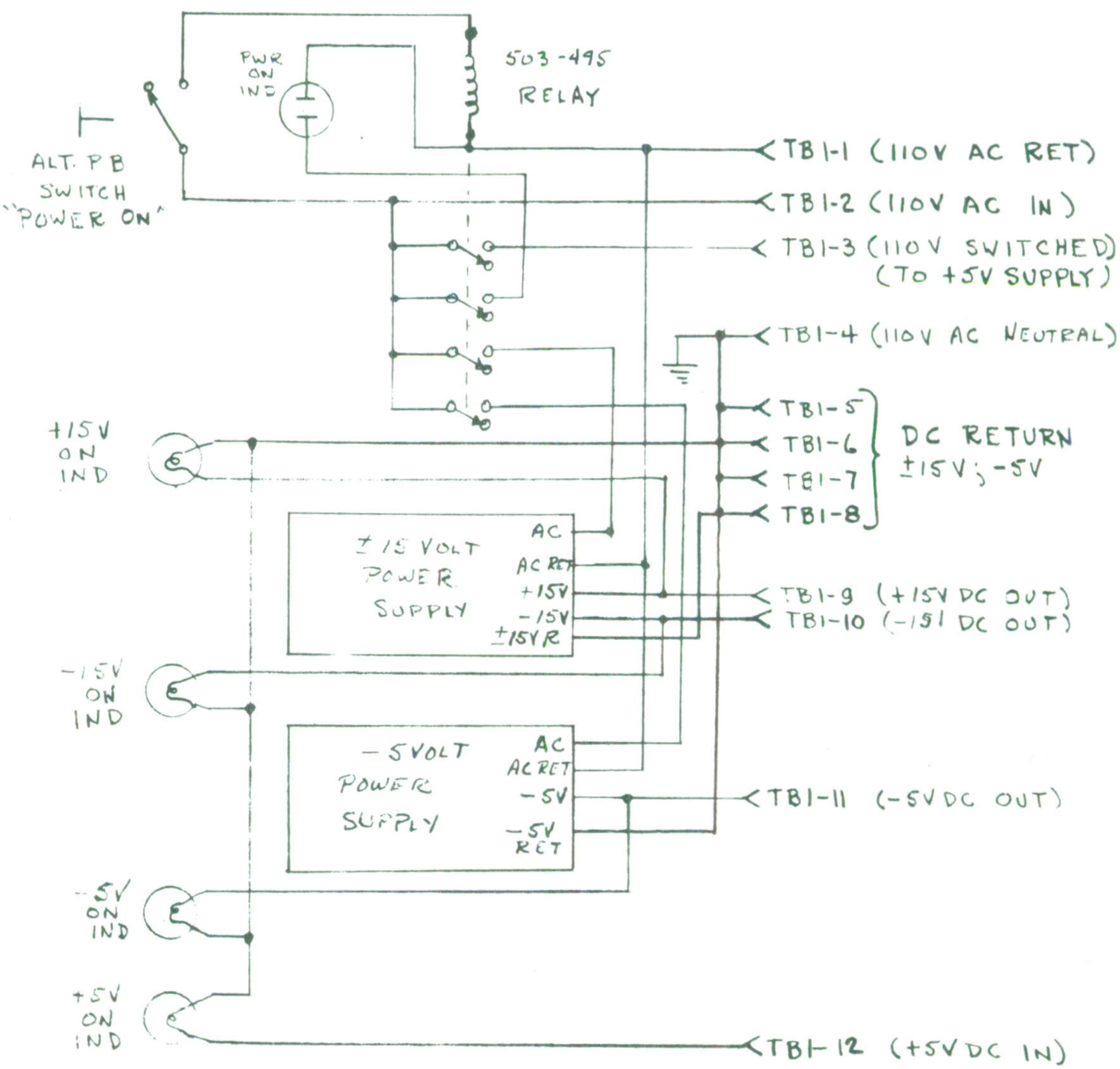


Fig. AI-32. Power supply control and status wiring sheet 1 of 1.

BLACK ANODIZED

BLANK PANELS REQUIRED

STANDARD 19" RACK

(1) 10.5"
(2) 5.25"
(1) 3.25"
(1) 8.75"
(1) 7.0"

THESE ARE IN ADDITION TO: -

TITLE PANEL	10.5"
MASTER CONTROL PANEL	5.25"
POWER SUPPLY CONTROL & STATUS	5.25"
INTERFACE PANEL	10.5" (PHENOLIC)
ALARM STATUS PANEL	7" --

Figure AI-33

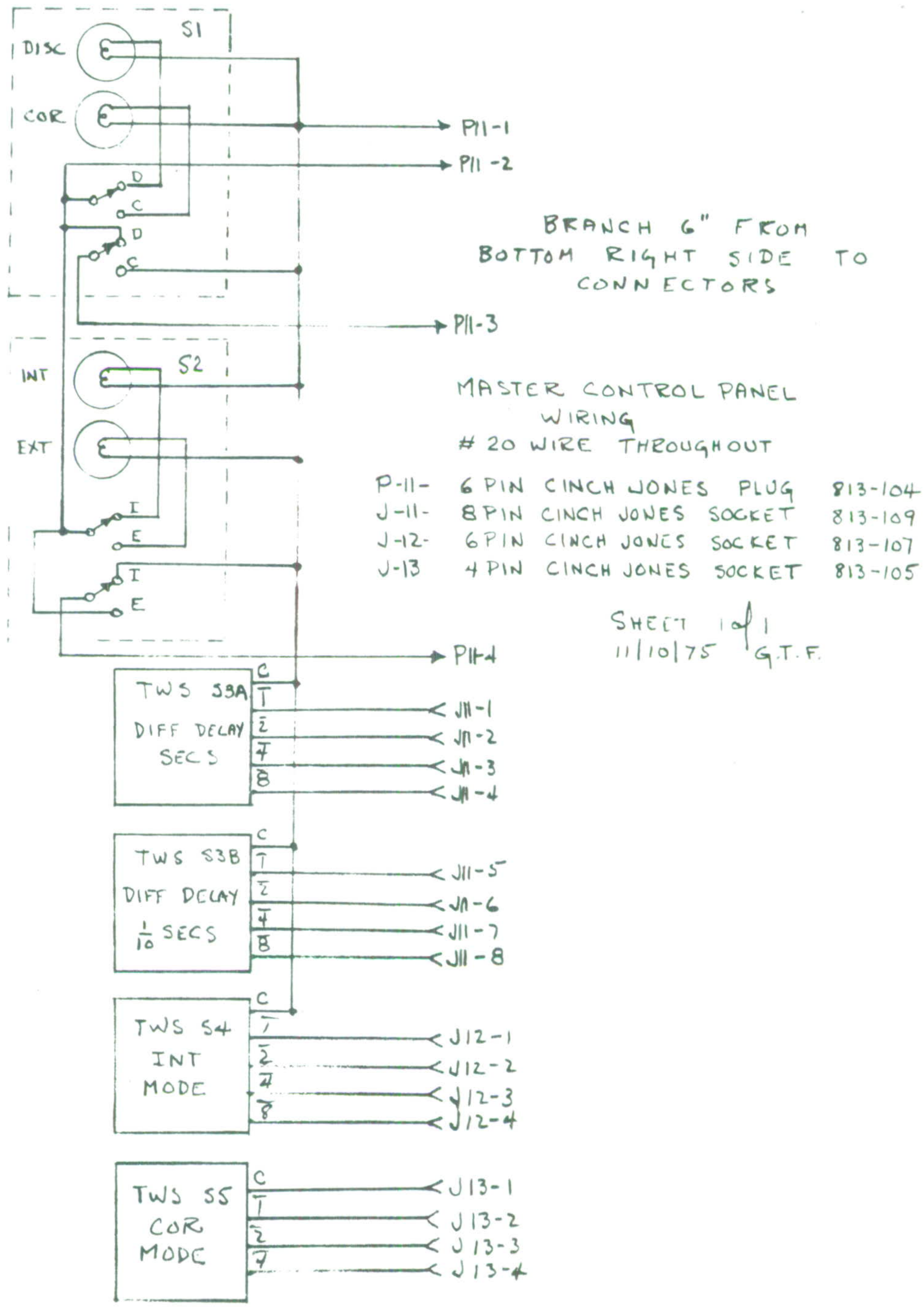

S1
DISC
COR
D
C
D
C
P11-1
P11-2
P11-3
S2
INT
EXT
I
E
I
E
P11-4
BRANCH 6" FROM BOTTOM RIGHT SIDE TO CONNECTORS
MASTER CONTROL PANEL WIRING
20 WIRE THROUGHOUT
P-11- 6 PIN CINCH JONES PLUG 813-104
J-11- 8 PIN CINCH JONES SOCKET 813-109
J-12- 6 PIN CINCH JONES SOCKET 813-107
J-13 4 PIN CINCH JONES SOCKET 813-105
SHEET 1 of 1
11/10/75 G.T.F.
TWS S3A
DIFF DELAY
SECS
C
1
2
4
8
J11-1
J11-2
J11-3
J11-4
TWS S3B
DIFF DELAY
1/10 SECS
J11-5
J11-6
J11-7
J11-8
TWS S4
INT
MODE
J12-1
J12-2
J12-3
J12-4
TWS S5
COR
MODE
J13-1
J13-2
J13-3
J13-4

Figure AI-34

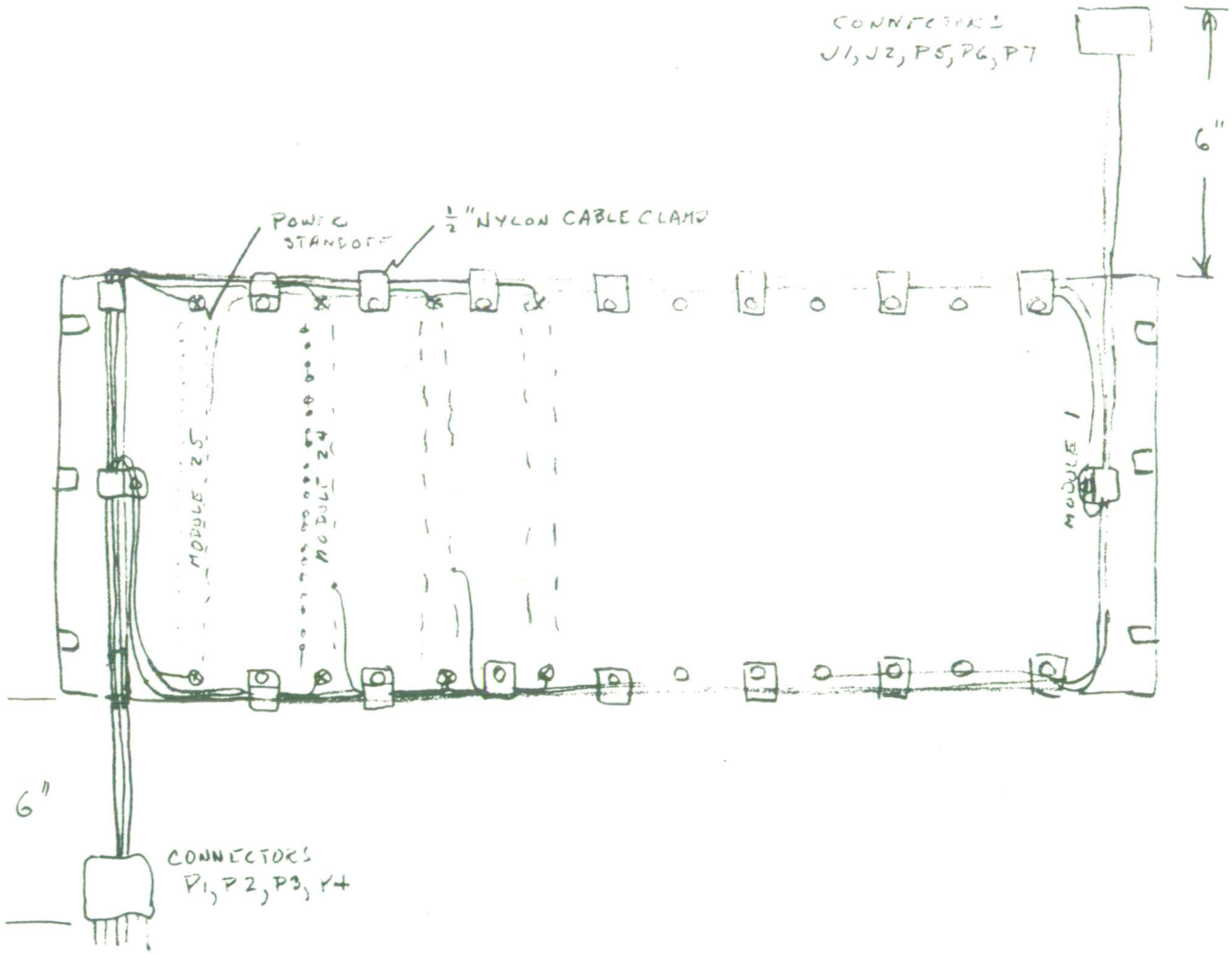


Fig. A-35. Module nest power; control and status cabling detail (not to scale).

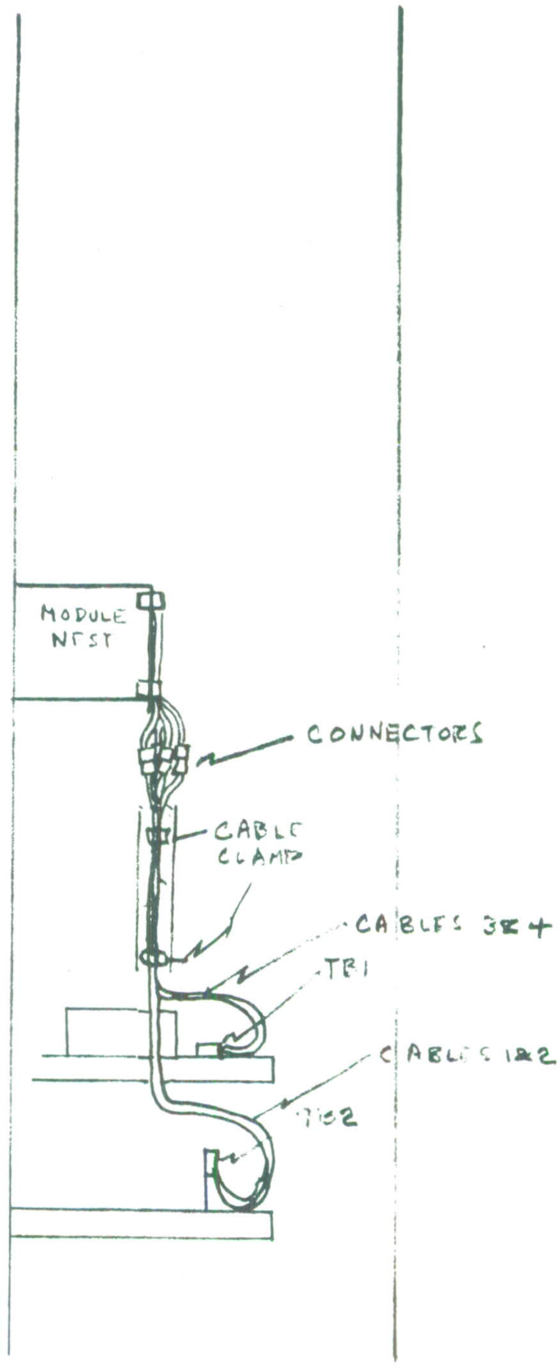


Fig. AI-36. Rack power cabling detail (not to scale).

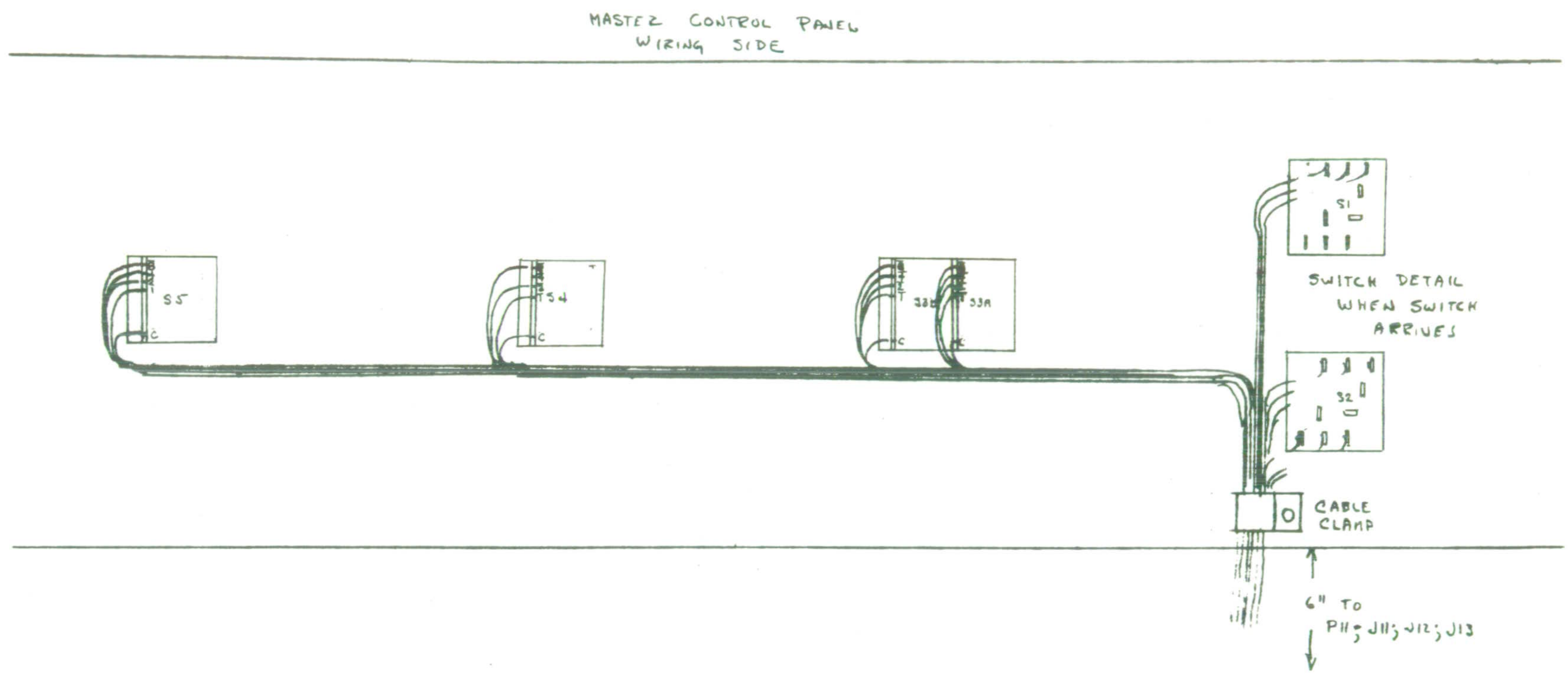


Fig. AI-37. Wiring Detail Master Control Panel

FIGURE AI-38

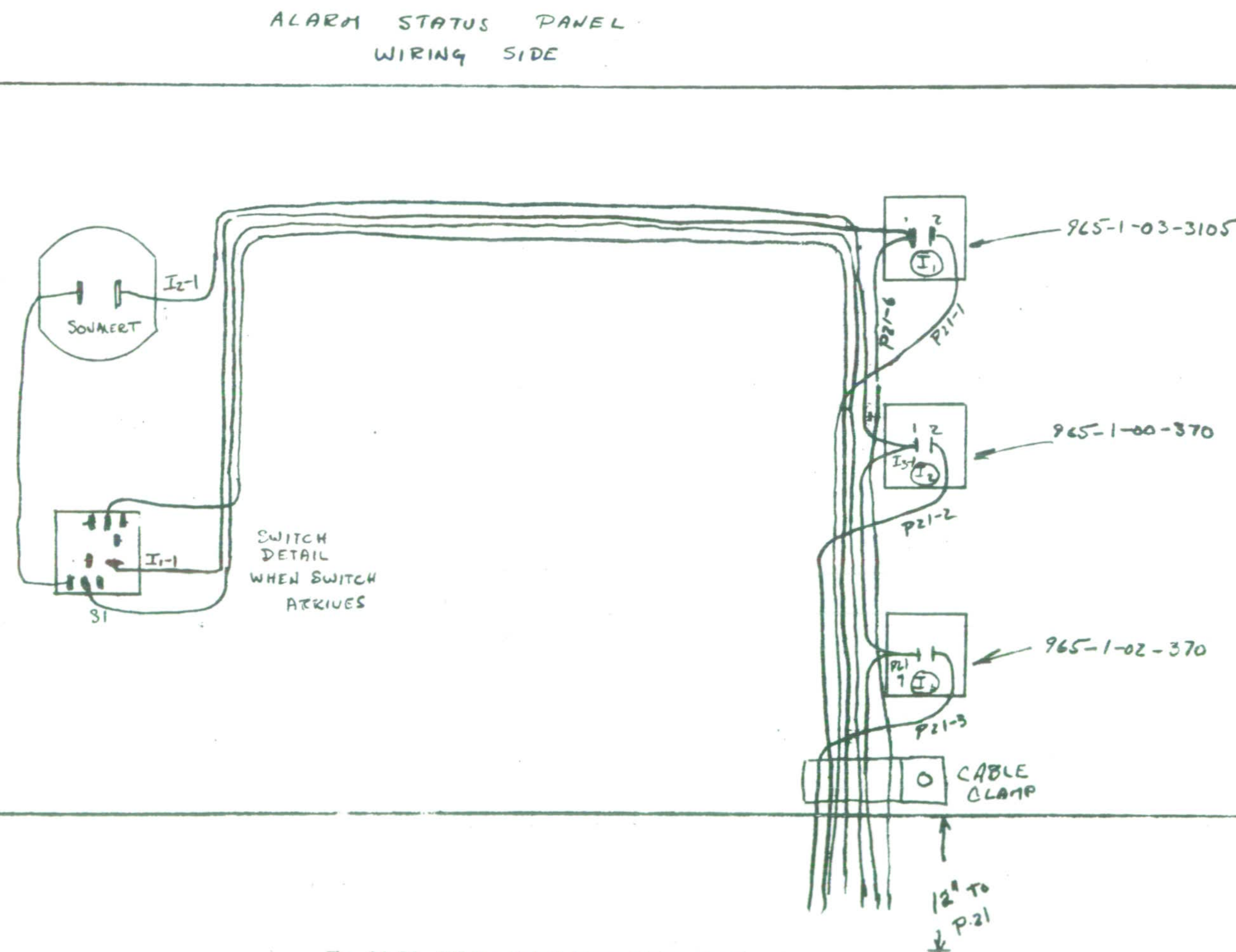


Fig. AI-38. Wiring Detail Alarm Status Panel.

MODULE NEST INTERCONNECT WIRING
POWER WIRING SHEET 1 OF 3 11/10/75 GTF

CONNECTOR	MOD /PIN	WIRE SIZE	NOTES
P1-1	1-+5V	#16	BRANCH OUT TO
P1-2	3-+5V		LEFT SIDE ON WIRING SIDE
P1-3	5-+5V		
P1-4	7-+5V		6" FROM BOTTOM OF
P1-5	1-+5RET		CHASSIS TO CONNECTORS
P1-6	3-+5RET		
P1-7	5-+5RET		
P1-8	7-+5RET		P1; P2 - 8 PIN PLUG 813-108
P2-1	9 +5V		P3; P4 - 6 PIN PLUG 813-106
P2-2	11 +5V		
P2-3	13 +5V		
P2-4	25 +5V		
P2-5	9 +5VRET		
P2-6	11 +5VRET		
P2-7	13 +5VRET		
P2-8	25 +5VRET		
P3-1	X -5V	X	OPEN - SPARE
P3-2	5 +15V		
P3-3	11 -15V		
P3-4	X -5VRET	X	OPEN - SPARE
P3-5	5 +15VRET		
P3-6	11 -15VRET		
P4-1	25 -5V		
P4-2	25 +15V		
P4-3	25 -15V		
P4-4	25 -5VRET		
P4-5	25 +15VRET		
P4-6	25 -15VRET		

Fig. AI-39.

MODULE NEST INTERCONNECT WIRING

CONTROL & STATUS WIRING SHEET 2 OF 3 11/10/75 G.T.F.

CONNECTOR	MOD/PIN	WIRE SIZE	NOTES
J1-1	11-59	#20	"SID TRK" ALARM STATUS P21-1
J1-2	5-104		READY " " P21-2
J1-3	5-44		FLASH ALARM " " P21-3
J1-4	5-105		AUDIO ALARM " " P21-4
J1-5	5-99		+5V RET " " P21-5
J1-6	5-106		+5V " " P21-6
J1-7	5-120		+15V " " P21-7
J2-1	11-110		+5RET MASTER CONT P11-1
J2-2	11-50		+5V " " P11-2
J2-3	11-49		DISC/COR " " P11-3
J2-4	11-111		INT/EXT " " P11-4
P5-1	5-99		COR C " " J13-1
P5-2	5-38		COR T " " J13-2
P5-3	5-39		COR 2 " " J13-3
P5-4	5-40		COR 4 " " J13-4
P6-1	11-42		INTEGRATE MODE 1 " " J12-1
P6-2	11-103		" " 2 " " J12-2
P6-3	11-43		" " 3 " " J12-3
P6-4	11-104		" " 4 " " J12-4
P7-1	11-39		DIFF DELAY SEC 1 J11-1
P7-2	11-40		" " " 2 " " J11-2
P7-3	11-99		" " " 4 " " J11-3
P7-4	11-100		" " " 8 " " J11-4
P7-5	11-44		" 1/10 SEC 1 " " J11-5
P7-6	11-105		" " " 2 " " J11-6
P7-7	11-106		" " " 4 " " J11-7
P7-8	11-101		" " " 8 " " J11-8

BRANCH TO RIGHT ON WIRING SIDE OF NEST

6" FROM TOP SIDE OF CHASSIS TO CONNECTORS SEE DETAIL

J1 - 8 PIN SOCKET 813-109
J2 - 6 PIN SOCKET 813-107
P5 - 4 PIN PLUG 813-104
P6 - 6 PIN PLUG 813-106
P7 - 8 PIN PLUG 813-108

CONTROL SIGNAL WIRING

Fig. AI-40.

MODULE NEST INTERCONNECT WIRING
SIGNAL WIRING SHEET 3 OF 3 11/10/75 GTF

CONNECTOR	MOD/PIN	WIRE SIZE	NOTES
BNC		RG188A	
	11-11	CETER	MAIN-H DR - FROM INTERFACE PANEL
	11-72	SHIELD	18" LONG
	11-12	CENTER	MON - H DR - FROM INTERFACE PANEL
	11-73	SHIELD	18" LONG
	11-16	CENTER	MAIN - V DR - FROM INTERFACE PANEL
	11-77	SHIELD	18" LONG
	11-17	CENTER	MON - V DR - FROM INTERFACE PANEL
	11-78	SHIELD	18" LONG
	11-26	CENTER	MAIN - BLANK FROM INTERFACE PANEL
	11-87	SHIELD	18" LONG
	11-28	CENTER	MON - BLANK FROM INTERFACE PANEL
	11-89	SHIELD	18" LONG
	11-34	CENTER	ODD FIELD PULSE FROM INTERFACE PANEL
	11-95	SHIELD	18" LONG
	11-41	CENTER	CONTROL SIGNAL TO INTERFACE PANEL
	11-102	SHIELD	18" LONG
	11-59	CENTER	MON. VIDEO FROM INTERFACE PANEL
	11-120	SHIELD	18" LONG
	11-61	CENTER	MAIN VIDEO FROM INTERFACE PANEL
	11-122	SHIELD	18" LONG
SPECIAL	11 - 1	TWISTED PAIR	SWITCHED CLOCK FROM INTERFACE PANEL
	11 - 62	SHIELDED	18" LONG
BNC	25-4	CENTER	LIVE VIDEO FROM INTERFACE PANEL
	25-65	SHIELD	18" LONG
	23-7	CENTER	MIXED LIVE VIDEO TO MONITOR
	23-68	SHIELD	24" LONG
	23-50	CENTER	MIXED X VIDEO TO MONITOR
	23-111	SHIELD	24" LONG

Fig. AI-41

RACK POWER SUPPLY HARNESS

SHEET 1 OF 1   11/10/75 G.T.F.

CABLE	CONNECTOR	TERMINAL	WIRE SIZE	NOTES	VIA
1	J101-1	TB2-4	#16	+5V TO MODULE -1	P1-1
	J101-2	TB2-5		" " " -3	P1-2
	J101-3	TB2-6		" " " -5	P1-3
	J101-4	TB2-13		" " " -7	P1-4
	J101-5	TB2-		+5V RET TO MODULE -1	P1-5
	J101-6	TB2-2		" " " -3	P1-6
	J101-7	TB2-3		" " " -5	P1-7
	J101-8	TB2-10		" " " -7	P1-8
2	J102-1	TB2-14		+5V TO MODULE -9	P2-1
	J102-2	TB2-15		" " " -11	P2-2
	J102-3	TB2-18		" " " -13	P2-3
	J102-4	TB2-19		" " " -25	P2-4
	J102-5	TB2-11		+5V RET TO MODULE -9	P2-5
	J102-6	TB2-12		" " " -11	P2-6
	J102-7	TB2-16		" " " -13	P2-7
	J102-8	TB2-17		" " " -25	P2-8
3	J103-1	TB1-11		-5V TO NOWHERE (SPARE)	P3-1
	J103-2	TB1-9		+15V TO MODULE -5	P3-2
	J103-3	TB1-10		-15V TO MODULE -11	P3-3
	J103-4	TB1-6		-5V RET TO NOWHERE (SPARE)	P3-4
	J103-5	TB1-7		+15V RET TO MODULE -5	P3-5
	J103-6	TB1-8		-15V RET TO MODULE -11	P3-6
4	J104-1	TB1-11		-5V TO MODULE-25	P4-1
	J104-2	TB1-9		+15V TO MODULE -25	P4-2
	J104-3	TB1-10		-15V TO MODULE -25	P4-3
	J104-4	TB1-6		-5V RET TO MODULE-25	P4-4
	J104-5	TB1-7		+15V RET TO MODULE 25	P4-5
	J104-6	TB1-8		-15V RET TO MODULE 25	P4-6
	TB1-12	TB2-13	#20	+5VDC TO INDICATOR	
	TB1-3	TB2-7	#16	110V AC SWITCHED TO +5V SUPPLY	
	TB1-1	TB2-8	#16	110V AC RETURN TO +5V SUPPLY	
	TB1-4	TB2-9	#16	110V AC NEUTRAL TO +5V SUPPLY	
	TB1-1	110V AC RETURN (LINE CORD)			
	TB1-2	110V AC (" ")			
	TB1-4	110V AC NEUTRAL (" ")			

FABRICATE CABLES ON BENCH

CABLE 1&2 - 3'

CABLE 3&4 - 2½'

Fig. AI-42

FROM PINS		FROM MOD 1 TO-M/P	FROM MOD 3 TO-M/P	FROM MOD 5 TO M/P	FROM MOD 7 TO M/P	FROM MOD 9 TO M/P	FROM MOD 11 TO M/P	FROM MOD 13 TO M/P	FROM MOD 25 TO M/P	
1	62			25-1 X 25-62			CL X CLR		∞ X ∞	
2	63			25-2 X 25-63					∞ X ∞	
3	64									
4	65							CH DIR ϕ EXT	∞ X ∞	
5	66							CV DIR ϕ EXT		
6	67	3-6 X 3-67	5-6 X 5-67	7-6 X 7-67	9-6 X 9-67	11-6 X 11-67	13-6 X 13-67	25-6 X 25-67	∞ X ∞	
7	68									
8	69									
9	70	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	
10	71									
11	72			9-31 X 9-92			H1 ϕ H1R	AR ϕ AR	-5V	
12	73			9-32 X 9-93			H2 ϕ H2R			
13	74							23-13 X 23-74	-5VR	
14	75									
15	76								-15V	
16	77			7-31 X 7-92			V1 ϕ V1R	∞ X ∞		
17	78			7-32 X 7-93			V2 ϕ V2R	∞ X ∞	-15VR	
18	79	+5R	+5R	+5R	+5R	+5R	+5R	+5R	+5R	
19	80							∞ X ∞		
20	81							∞ X ∞		
21	82	3-21 X 3-82	5-21 X 5-82	7-21 X 7-82	9-21 X 9-82	11-21 X 11-82	13-21 X 13-82	25-21 X 25-82	∞ X ∞	
22	83	3-22 X 3-83	5-22 X 5-83	7-22 X 7-83	9-22 X 9-83	9-22 X 9-83	13-22 X 13-83	25-22 X 25-83	∞ X ∞	
23	84						25-23 X 25-84		∞ X ∞	
24	85						23-24 X 23-85		∞ X ∞	
25	86						-15V			
26	87			∞ ∞			B1 ϕ B1R			
27	88	9	9	9	9	9	9	9	9	
28	89			∞ ∞			B2 ϕ B2R		+15V	
29	90						-15VR			
30	91								+15VR	
31	92	5-31 X 5-92	5-26 X 5-87	∞ X ∞	∞ X ∞	∞ X ∞	S1 S1R			
32	93	5-32 X 5-93	5-28 X 5-89	∞ X ∞	∞ X ∞	∞ X ∞	S2 S2R			
33	94						S-TRK ϕ STRK-R			
34	95						OFP ϕ OFPR			
35	96	5-35 X 5-96	5-41 X 5-102	∞ X ∞	∞ X ∞	∞ X ∞				
36	97	18	18	18	18	18	18	18	18	
37	98	3-37 X 3-98	7-37 X 7-98	∞ X ∞	9-37 X 9-98	11-37 X 11-98	13-37 X 13-98			
38	99			M1 MC			SEC4			
39	100			M2			SEC1 SEC8			
40	101			M4			SEC2 SEC8			
41	102			∞ ∞			DLC ϕ DLCR			
42	103	5-37 X 5-98	5-42 X 5-103	∞ ∞	∞ X ∞	∞ X ∞	INT4 INT2			
43	104			READY			INT1 INT8			
44	105			F ALM A ALM			SEC.1 SEC.2			
45	106	27	27	27	27	27	27 SEC.4	27	37	
46	107						CV CVR			
47	108			11-47 X 11-108			∞ X ∞			
48	109			11-48 X 11-109			∞ X ∞			
49	110						CYC2 CYC3			
50	111						CYC1 INT/EXT			
51	112			7-35 X 7-96			13-16, 25-51 X 13-77, 25-112		∞ X ∞	
52	113			7-42 X 7-103			13-17, 25-52 X 13-78, 25-113		∞ X ∞	
53	114						13-19, 25-53 X 13-80, 25-114		∞ X ∞	
54	115	36	36	36	36	36	36	36	36	
55	116						13-20, 25-55 X 13-81, 25-116		∞ X ∞	
56	117			9-35 X 9-96						
57	118			9-42 X 9-103				23-57 X 23-118		
58	119									
59	120			+15V +15VR			J1-1			
60	121			11-60 X 11-121			∞ X ∞			
61	122			+15VR						
		MEM 1&2	MEM 3&4	CORRELATOR	MEM 5&6	MEM 7&8	INTERFACE	CURSOR G	CFAR DET	VIDEO MIX

WHT X BLK		TWISTED PAIR
CTR ϕ SHLD		COAX
∞		(FINAL CONN)/(NO CONN)
M-P	N	TO-(MODULE-PIN) / TO-(SAME MODULE-PIN)

WIRING PROCEEDS FROM LEFT TO RIGHT
ALL WIRES CALLED OUT ONLY ONCE

Fig. AI-43 CFAR Detector & Correlator Backplane Wiring.

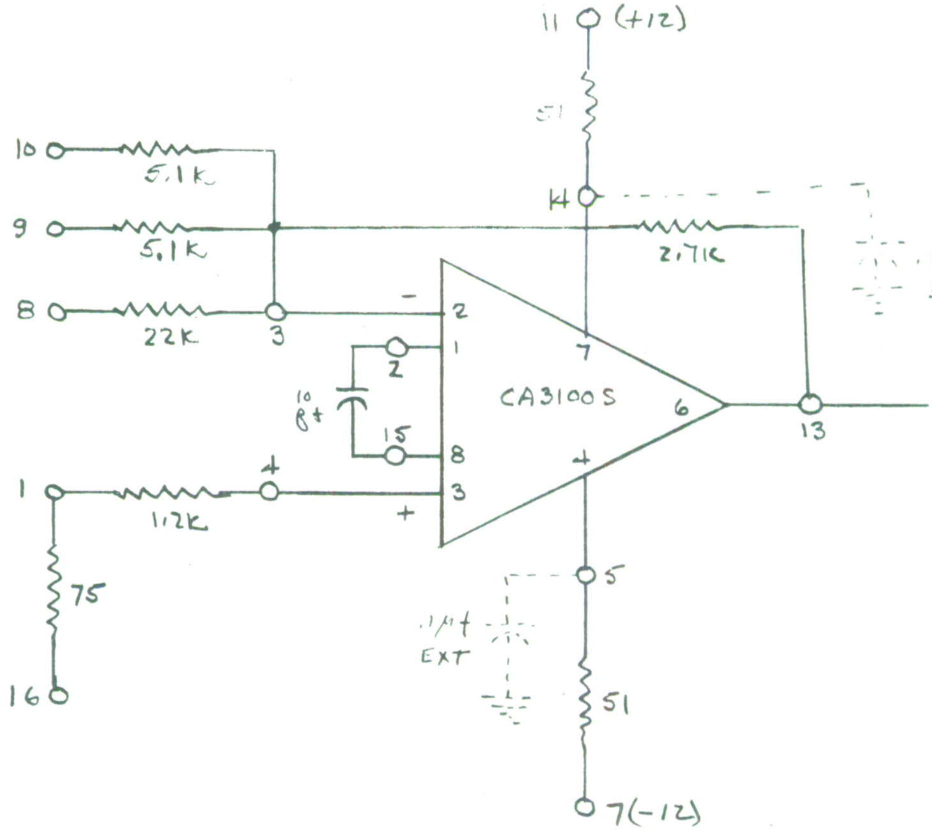


Fig. AII-1. (2 x) Vid amp on component carrier.

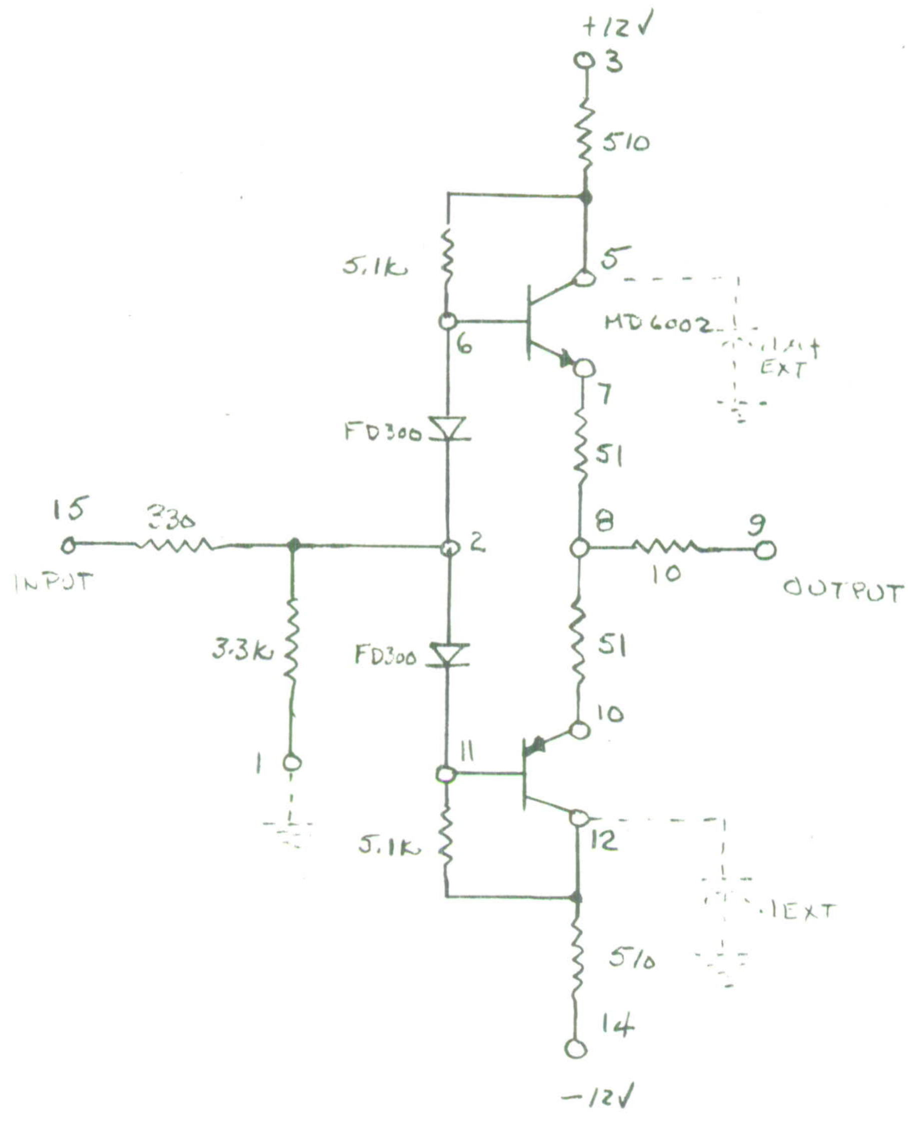


Fig. AII-2. 75 Ω Video line driver on component carrier.

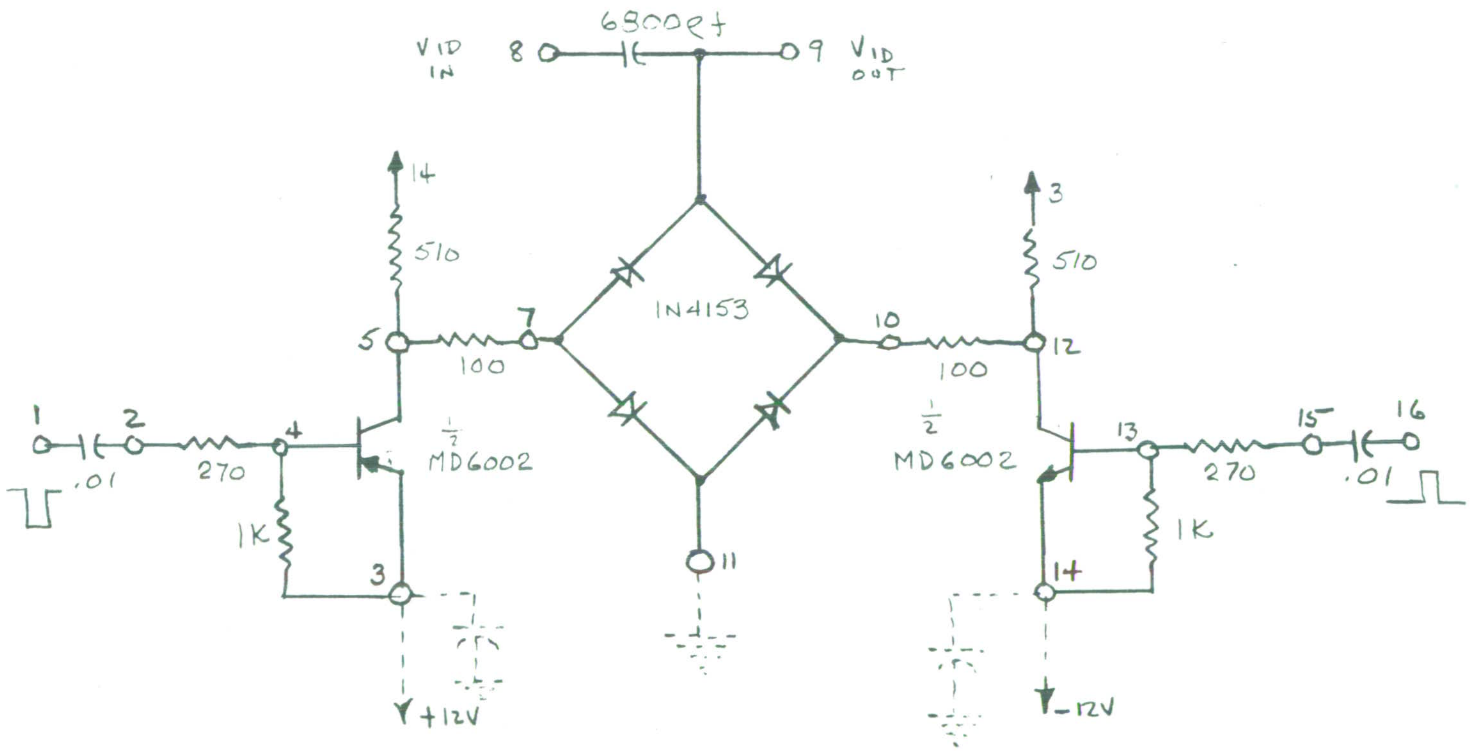


Fig. AII-3. Video clamp circuit.

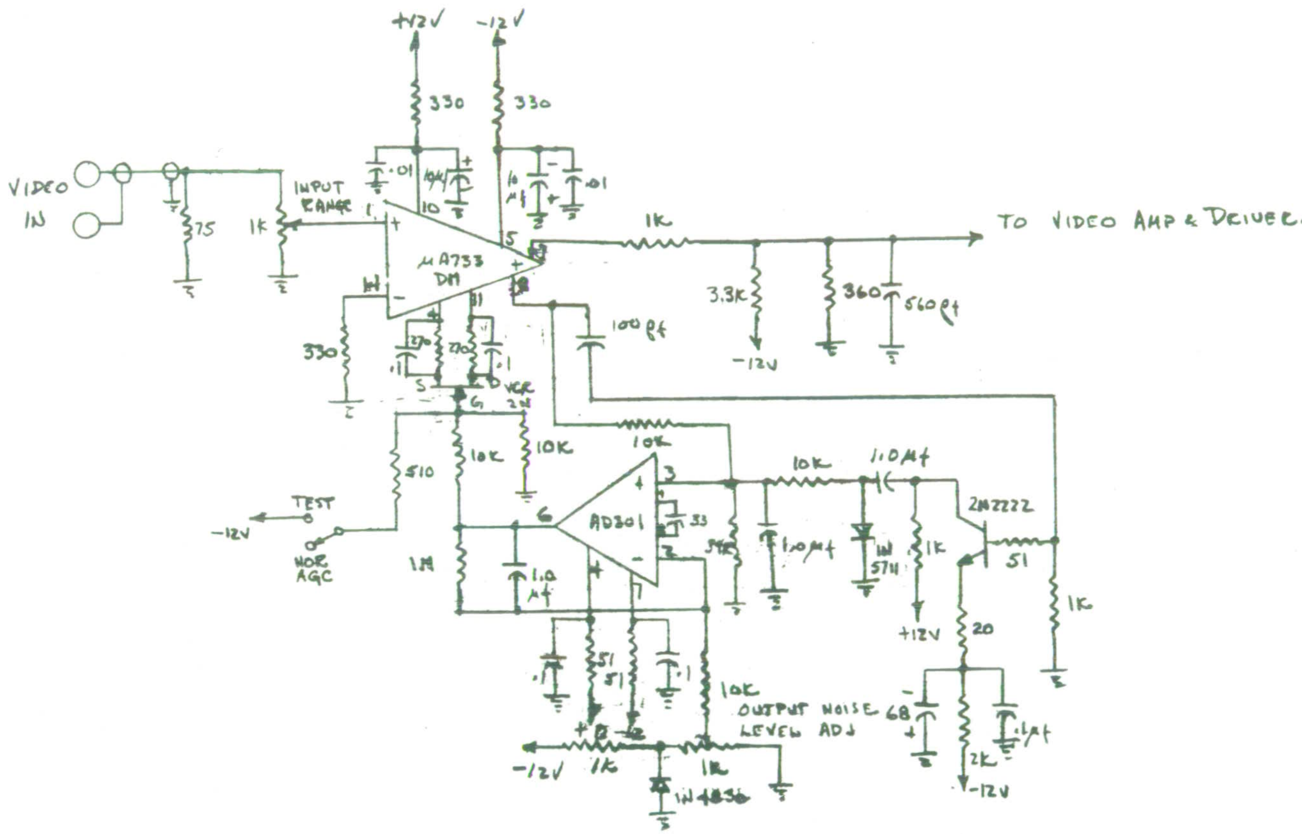
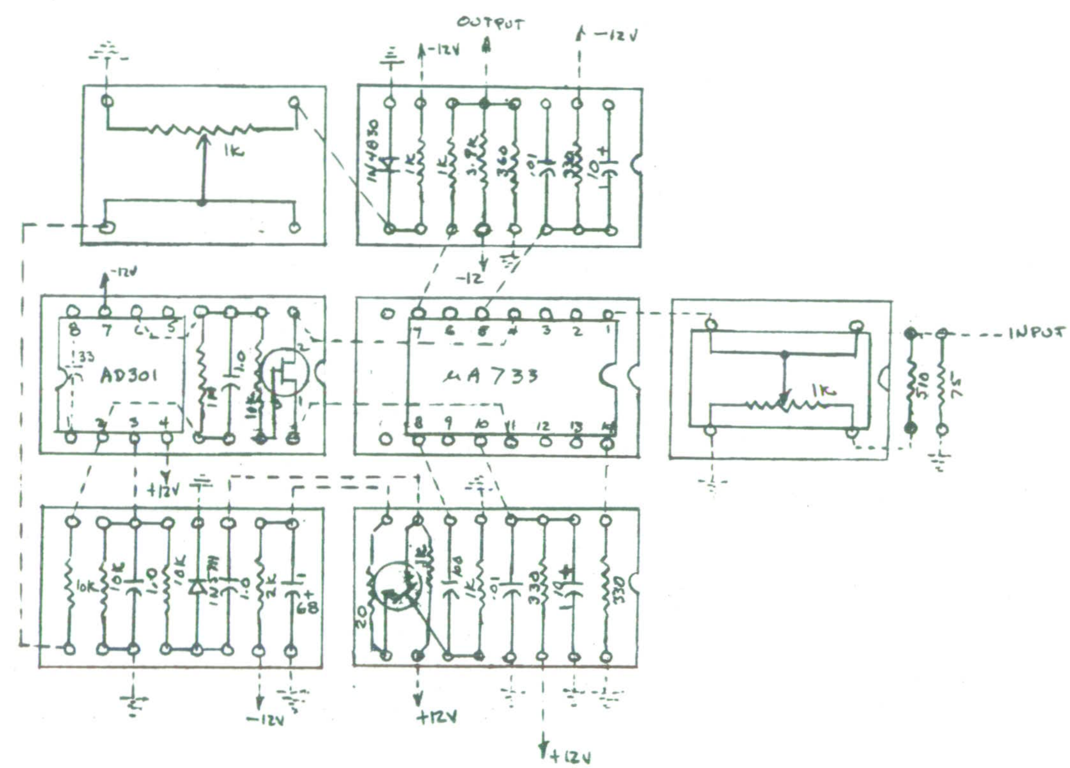


Fig. A11-4. Video Noise AGC (Sheet 1 of 2).



VID PROC #1

H10	H9	
F10	F9	F8
E10	E9	

VID PROC #2

C6; F7	C5; F6	
B6; E7	B5; E6	B4; E5
A6; D7	A5; D6	

Fig. AII-5. Video Noise AGC (Sheet 2 of 2) Circuit Layout Component Side.

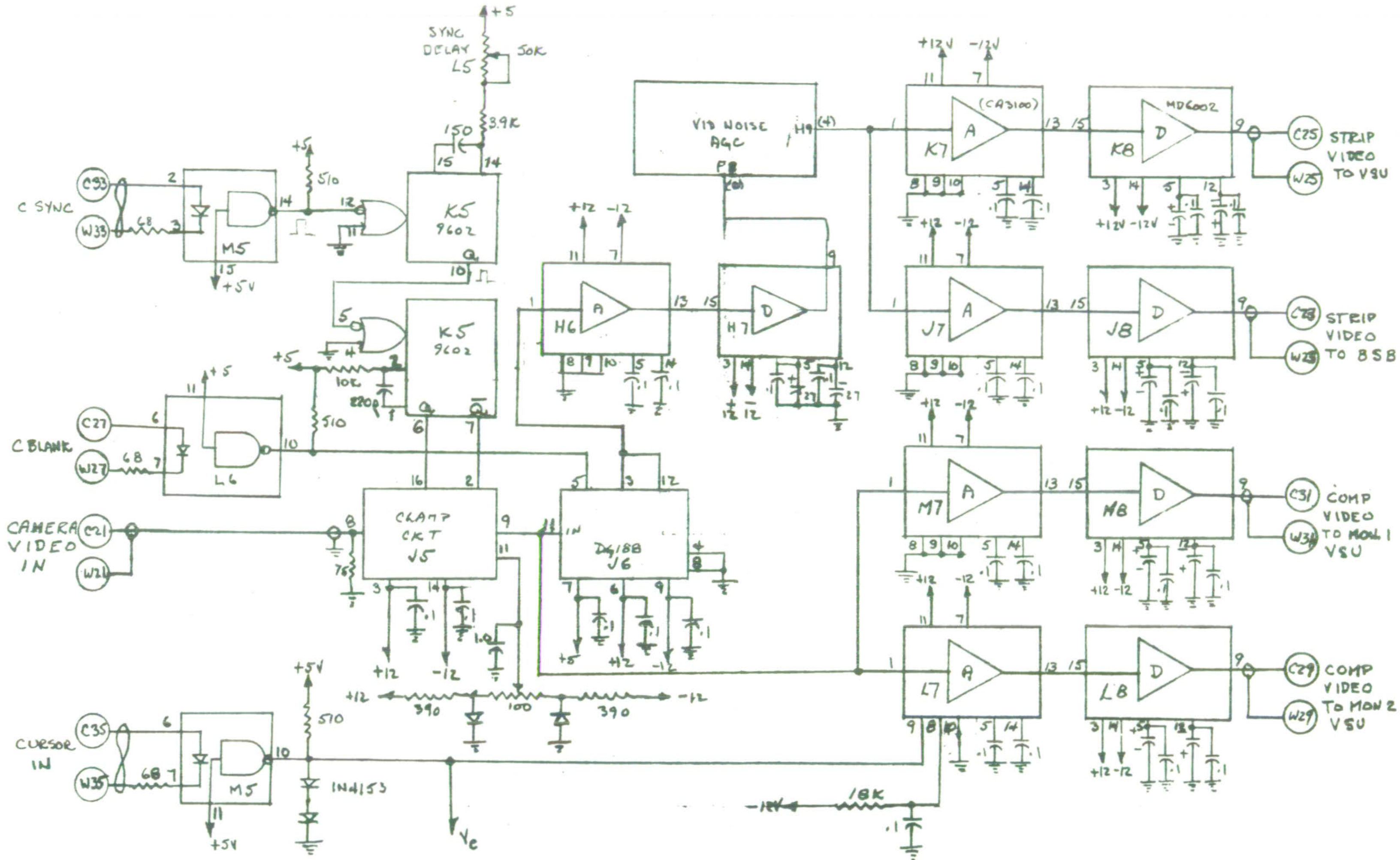


Fig. AII-6. Video Processor Number 1 Camera Video Distribution (Sheet 1 of 3).

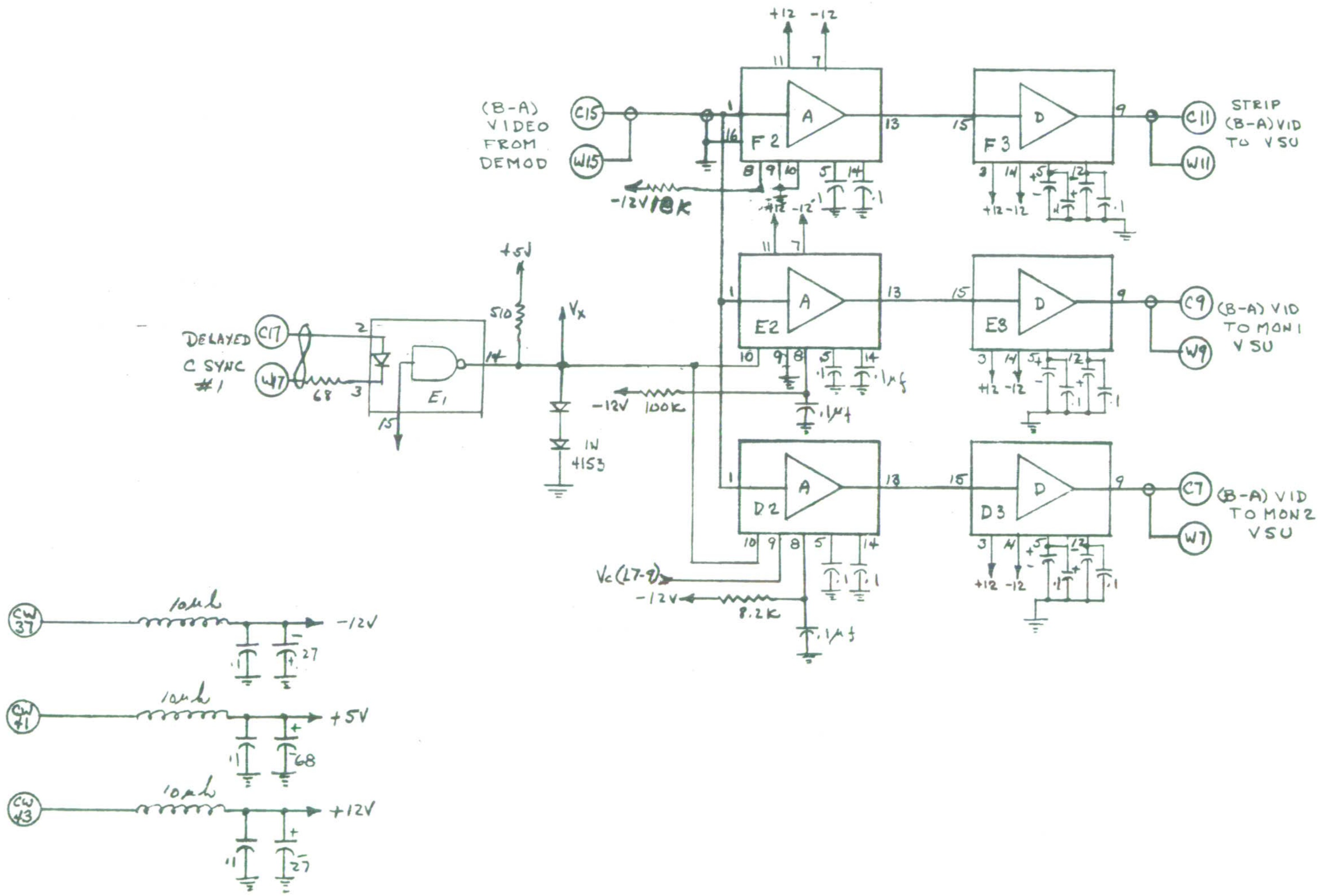


Fig. A11-7. Video Processor Number 1 (B-A) Video Distribution (Sheet 2 of 3).

1) Connect All Even Pins to Ground
2) Connect "Ocean Planes" to Ground
3) Wiring Side – Connect A thru M "Island Planes" to –12VDC
4) Component Side – Connect A thru M "Island Planes" to +12VDC
5) Wiring Side – Connect "M & J" Perimeter to +5V
6) Component Side – Connect "A" Perimeter to +5V
7) Connect All Outer Perimeter to Ground

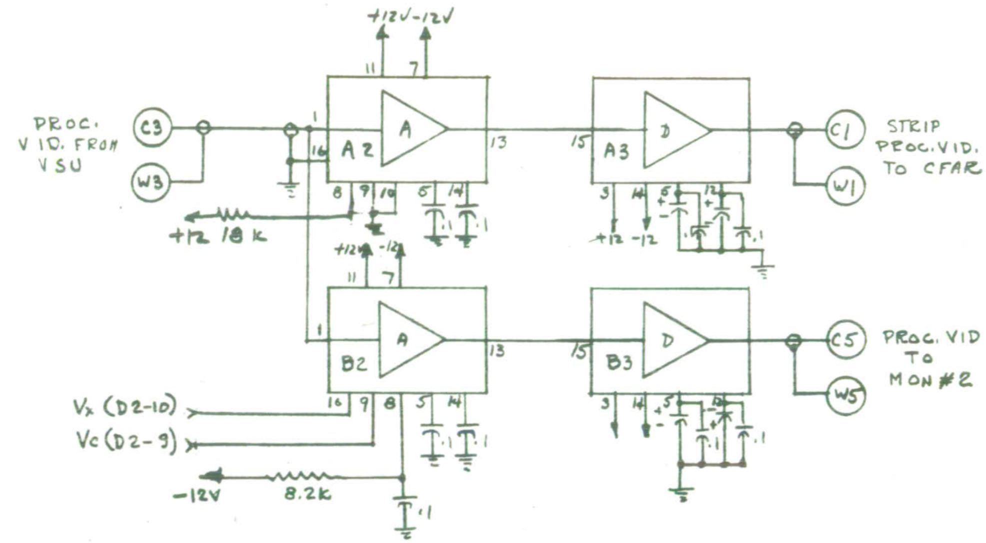


Fig. AII-8. Video Processor Number 1 Processed Video Distribution (Sheet 3 of 3).

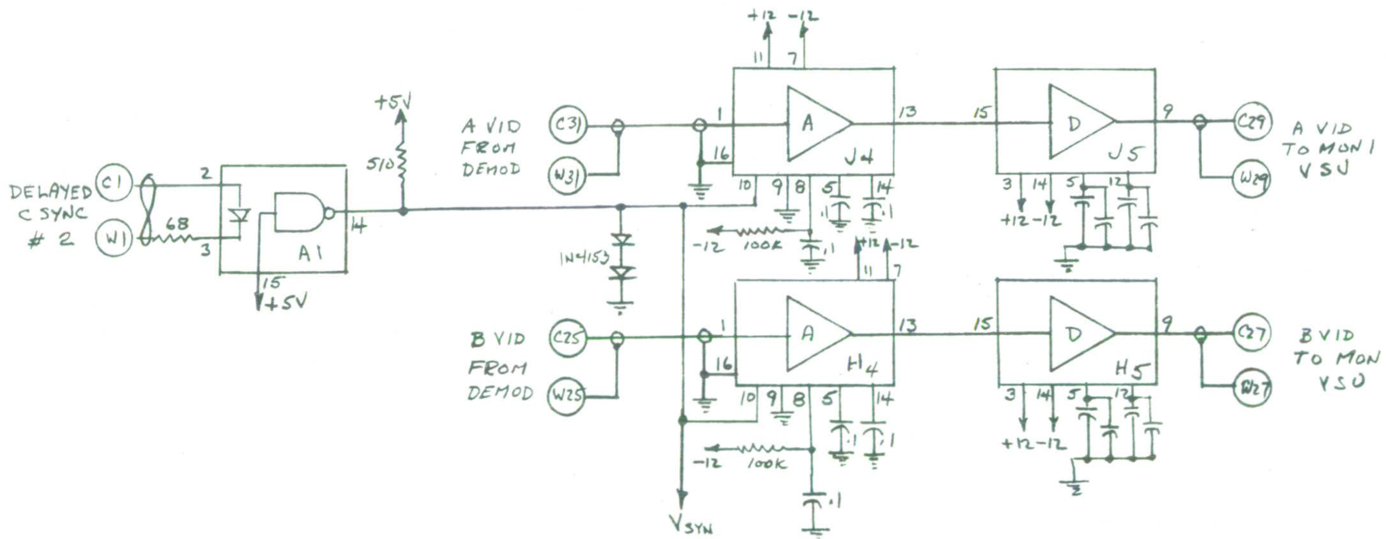


Fig. AII-9. Video Processor Number 2 A & B Video Distribution (Sheet 1 of 2)

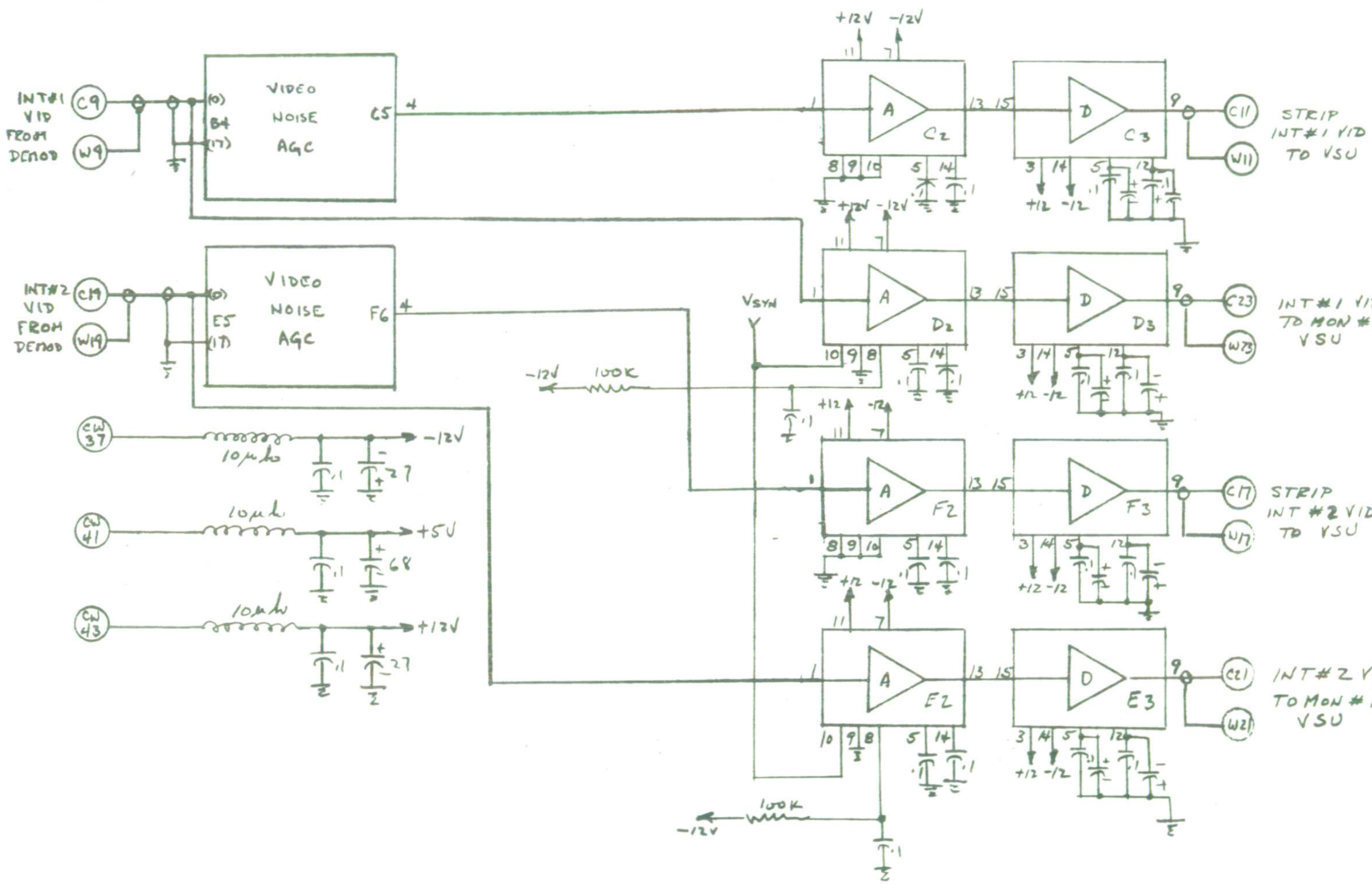


Fig. AII-10. Video Processor Number 2 Int. Vid. Dist. (Sheet 2 of 2)

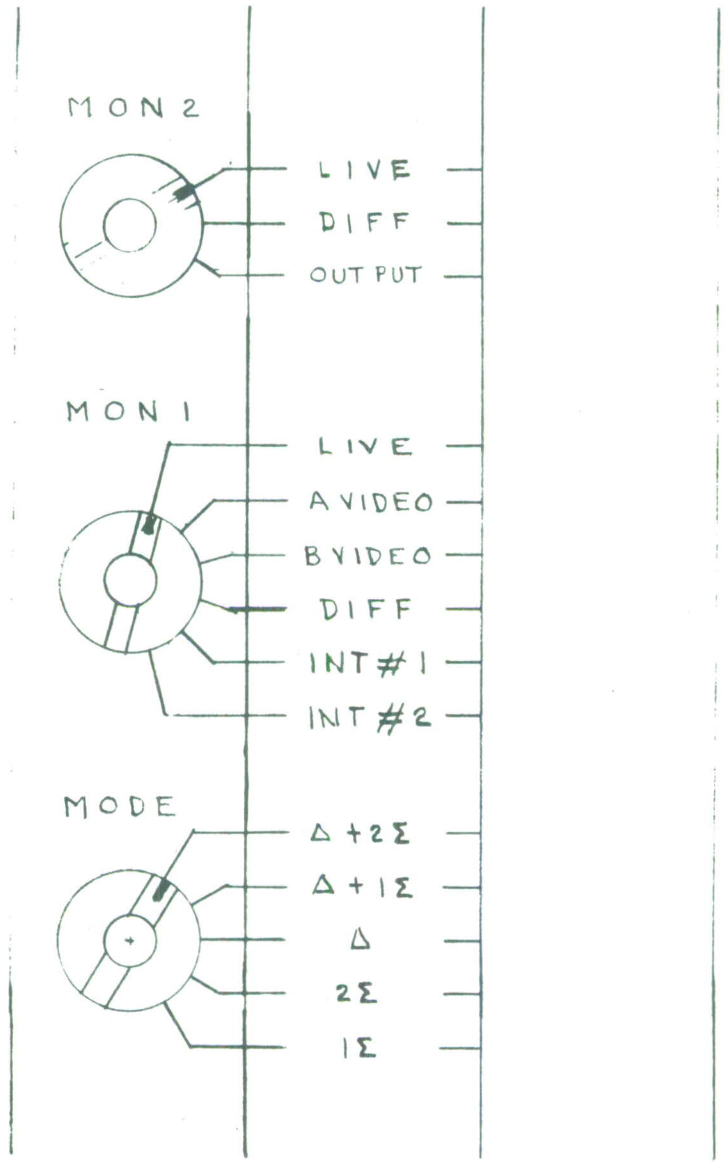


Fig. AII-11. Video switching unit front panel engraving.

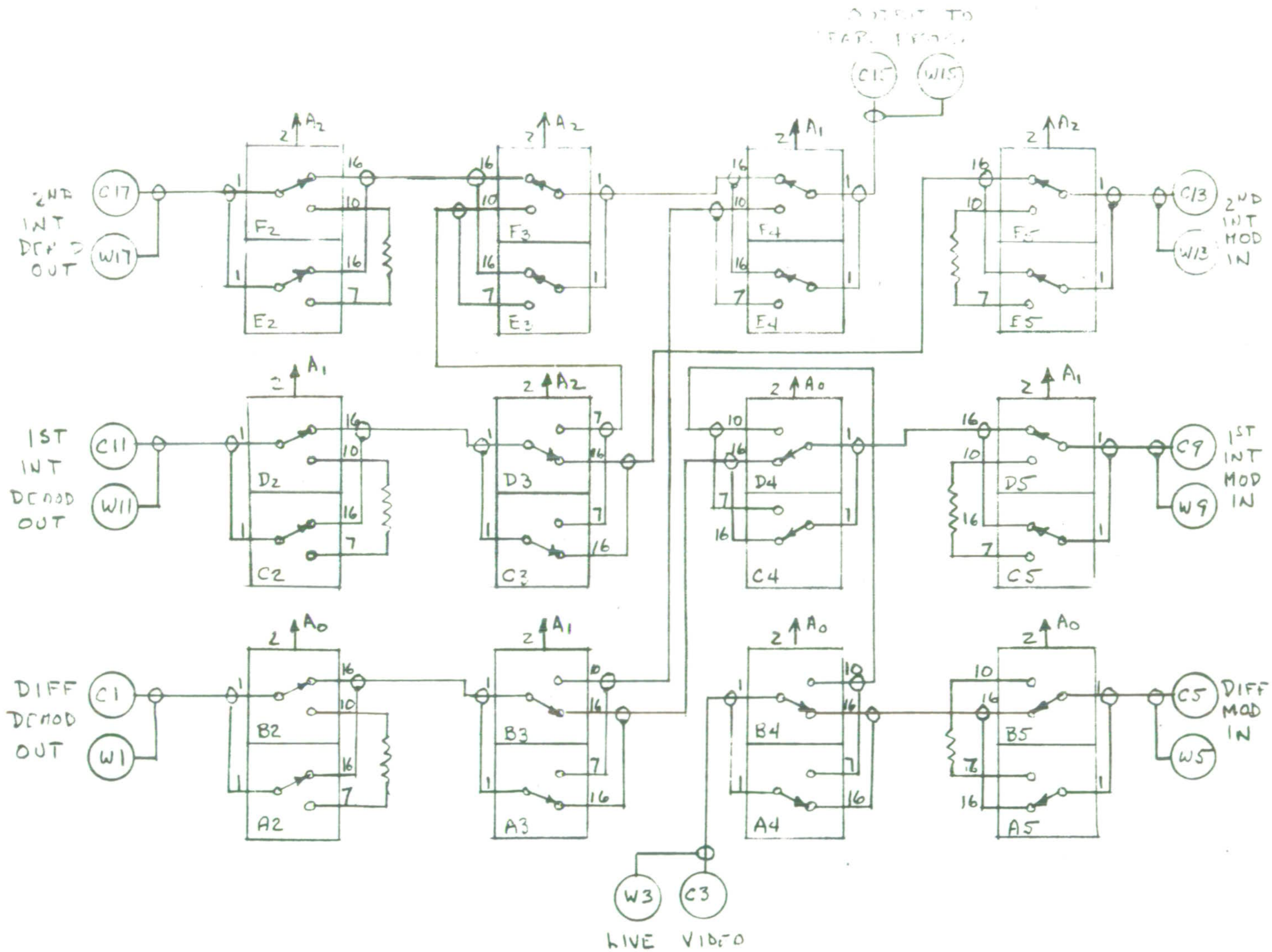


Fig. AII-12. Video Sw unit config. Sw schematic.

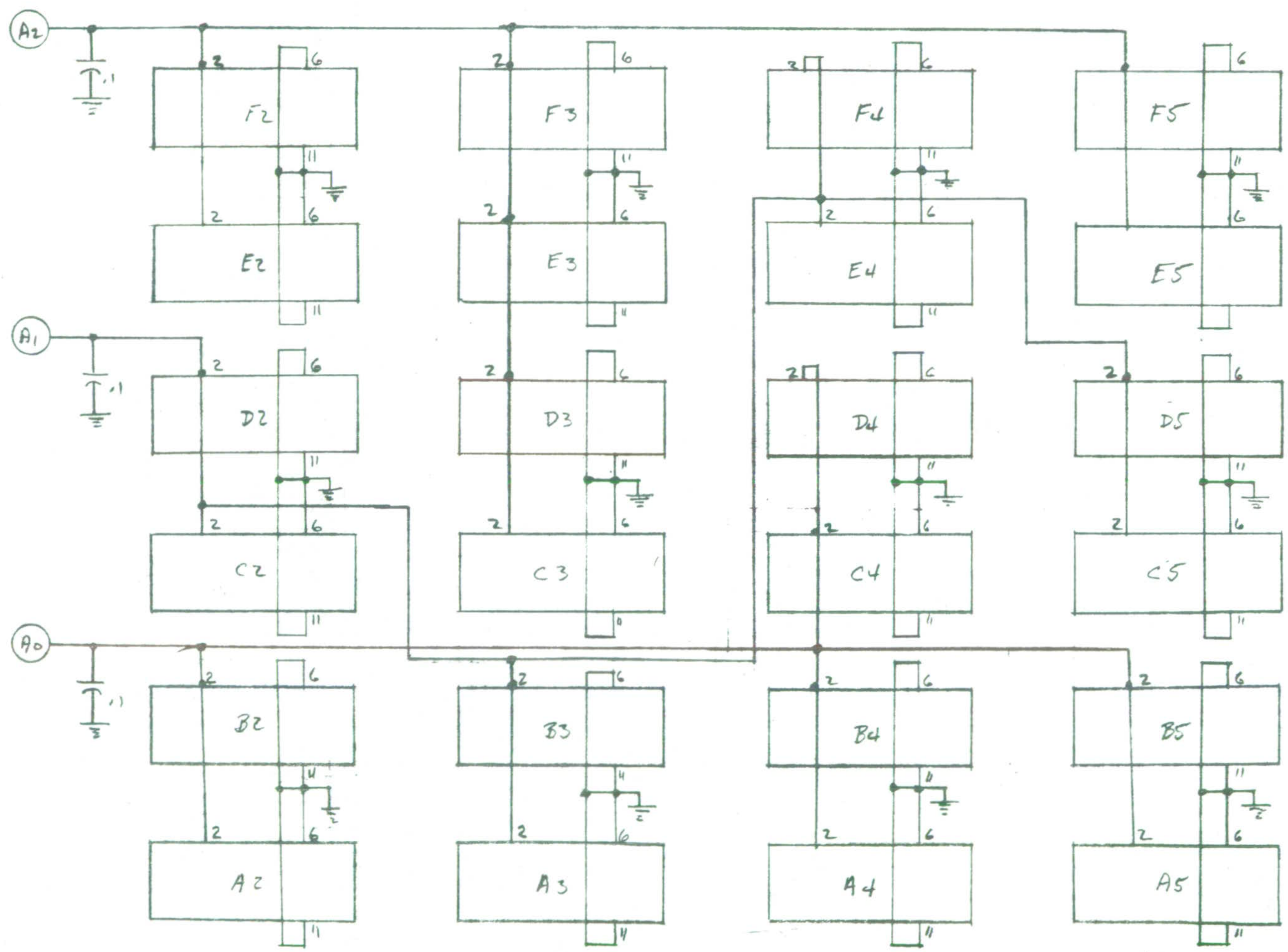


Fig. AII-13. Video Sw Unit Configuration Switching Control Wiring (Sheet 1 of 5).

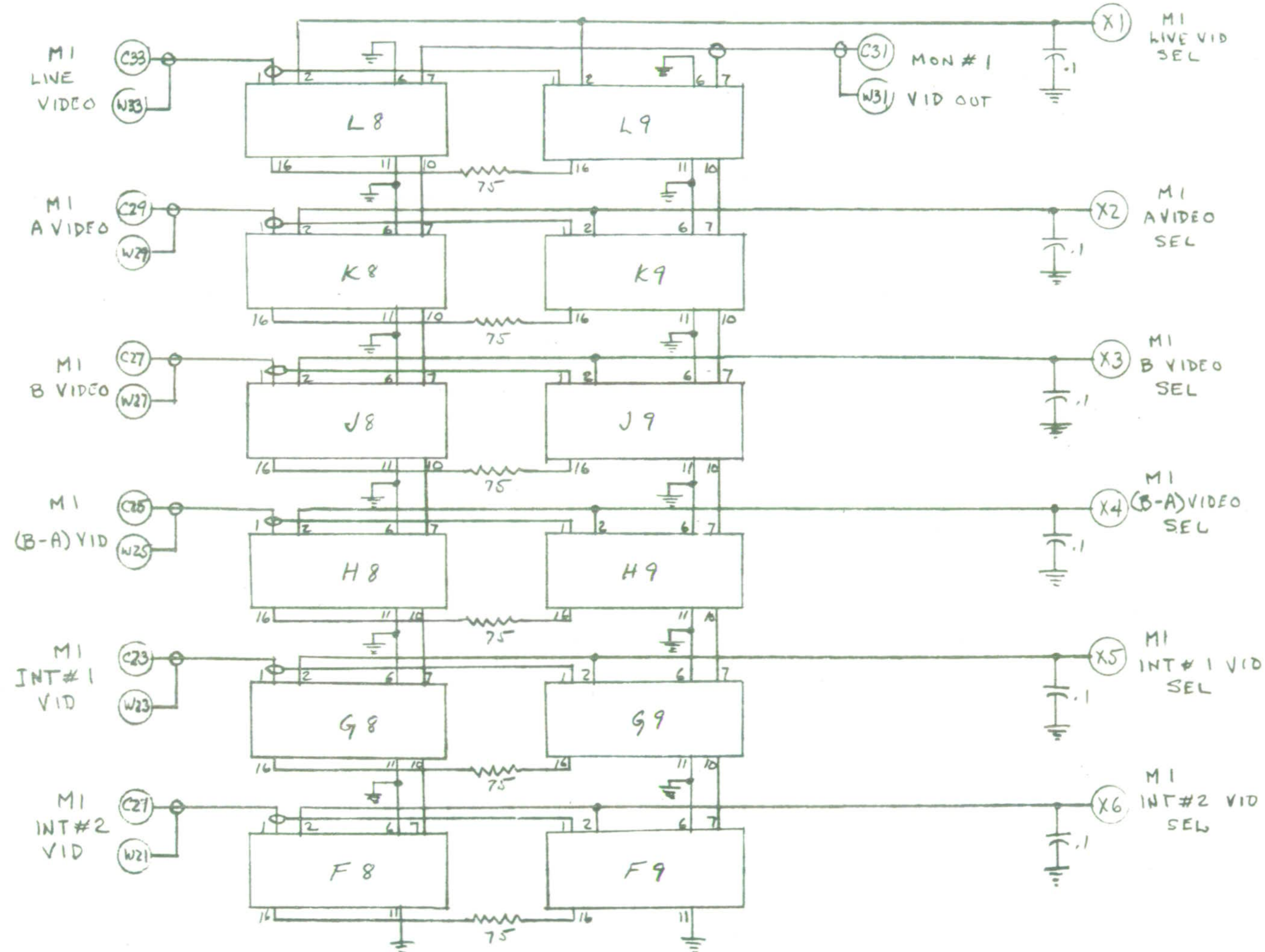
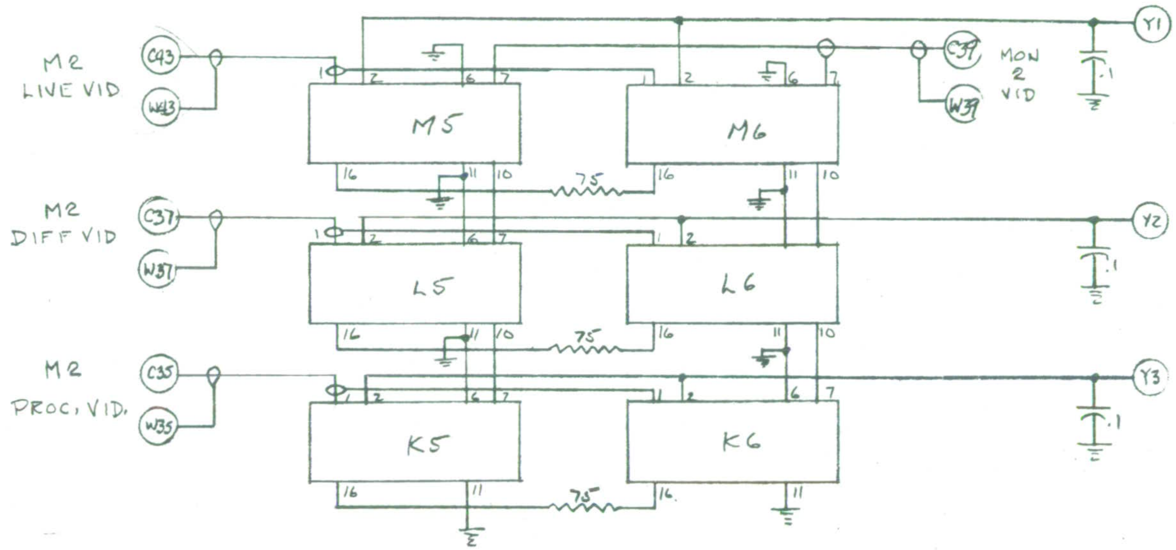


Fig. A11-14. Video Sw Unit Monitor Number 1 Video Switching (Sheet 3 of 5).



C/W 41 → +5V

GROUND ALL EVEN PINS

DO NOT GROUND COAX SHIELDS

CONNECT ALL METALIZED AREAS TO GROUND EXCEPT FOR ONE EDGE STRIP

USE ONE EDGE STRIP TO RUN +5V TO SWITCHES

Fig. AII-15. Video Switching Unit Monitor Number 2 Video Switching (Sheet 4 of 5).

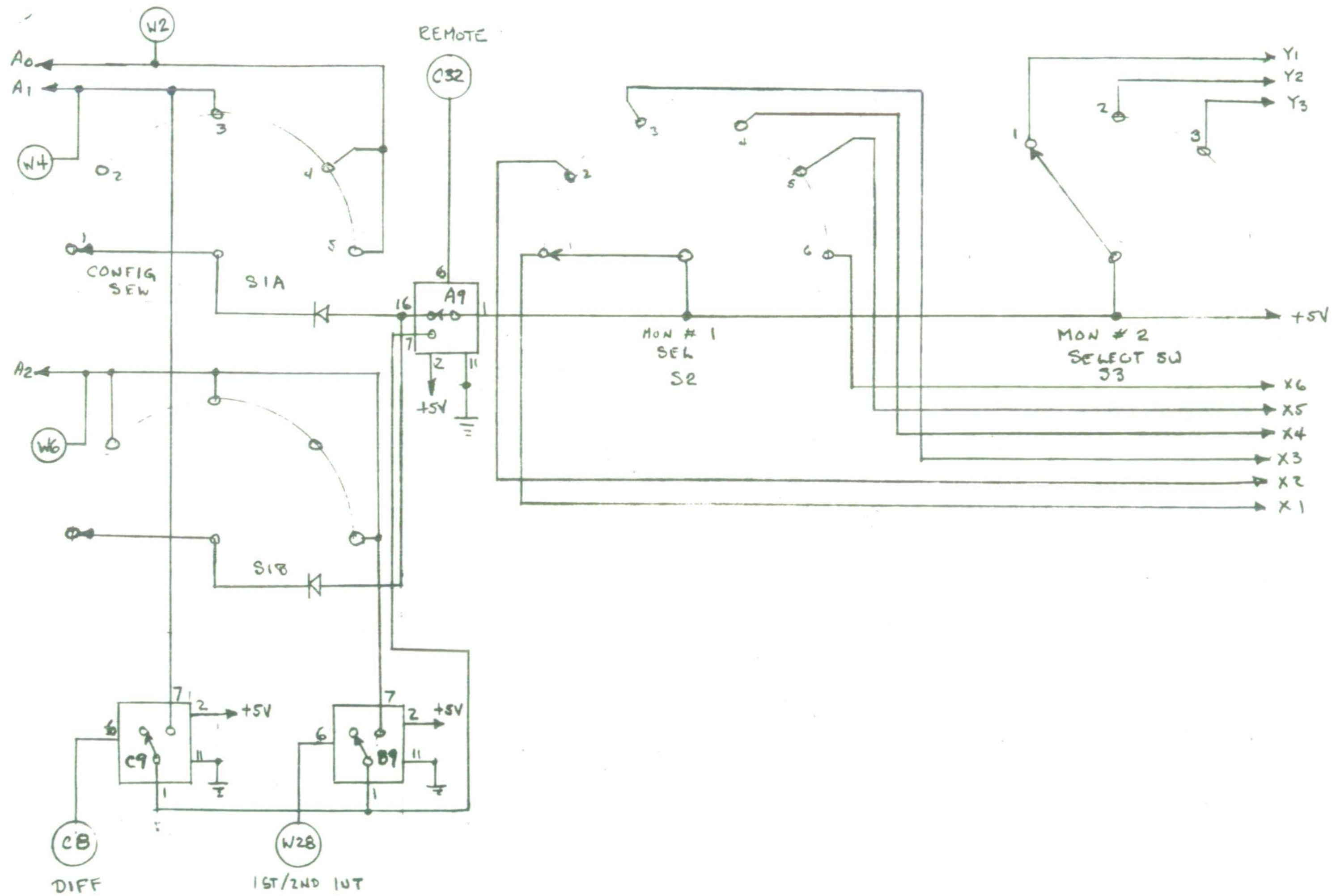


Fig. AII-16. Video Switching Unit Front Panel Switching (Sheet 5 of 5).

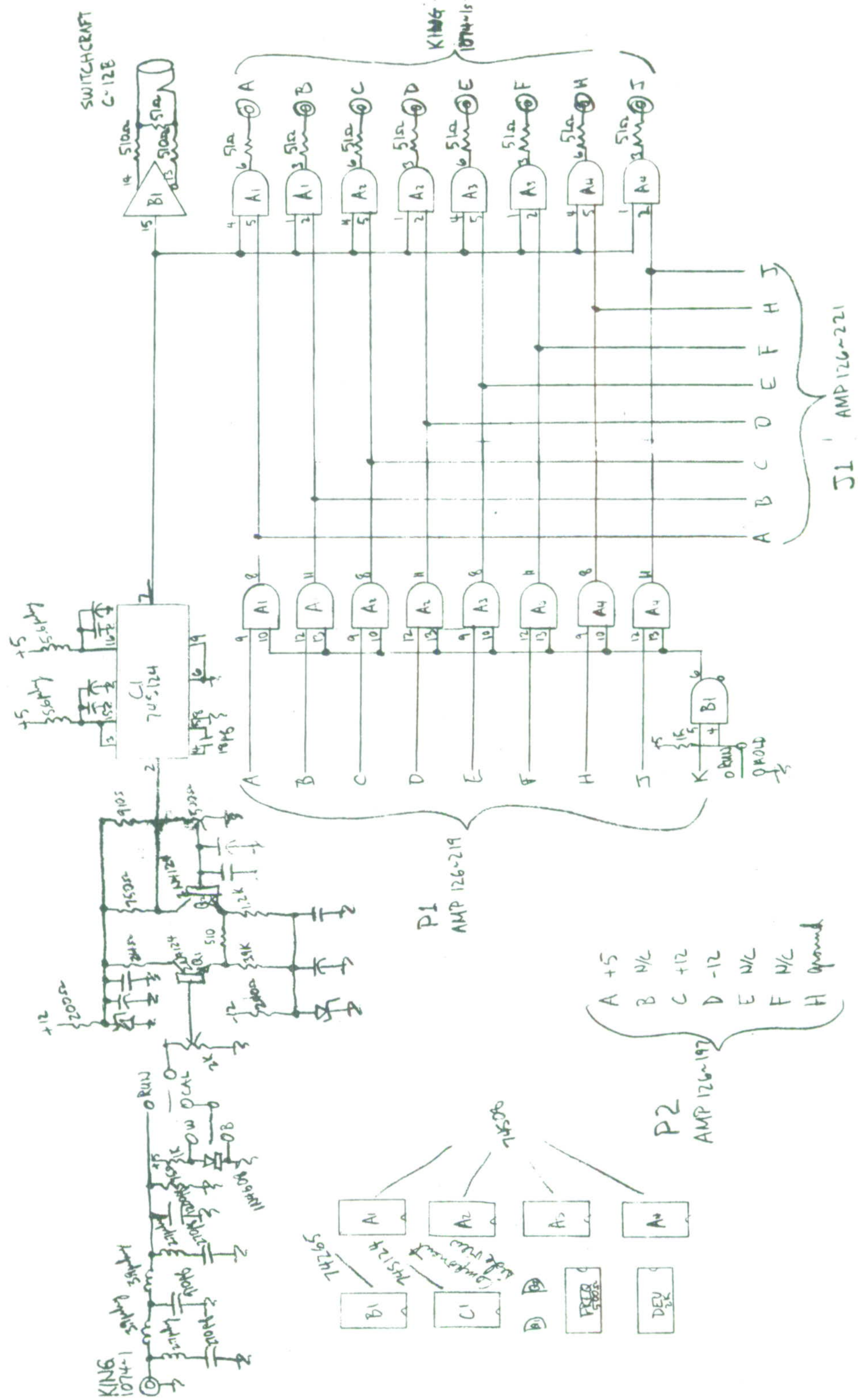


Fig. A11-17. Modulator & Gating.

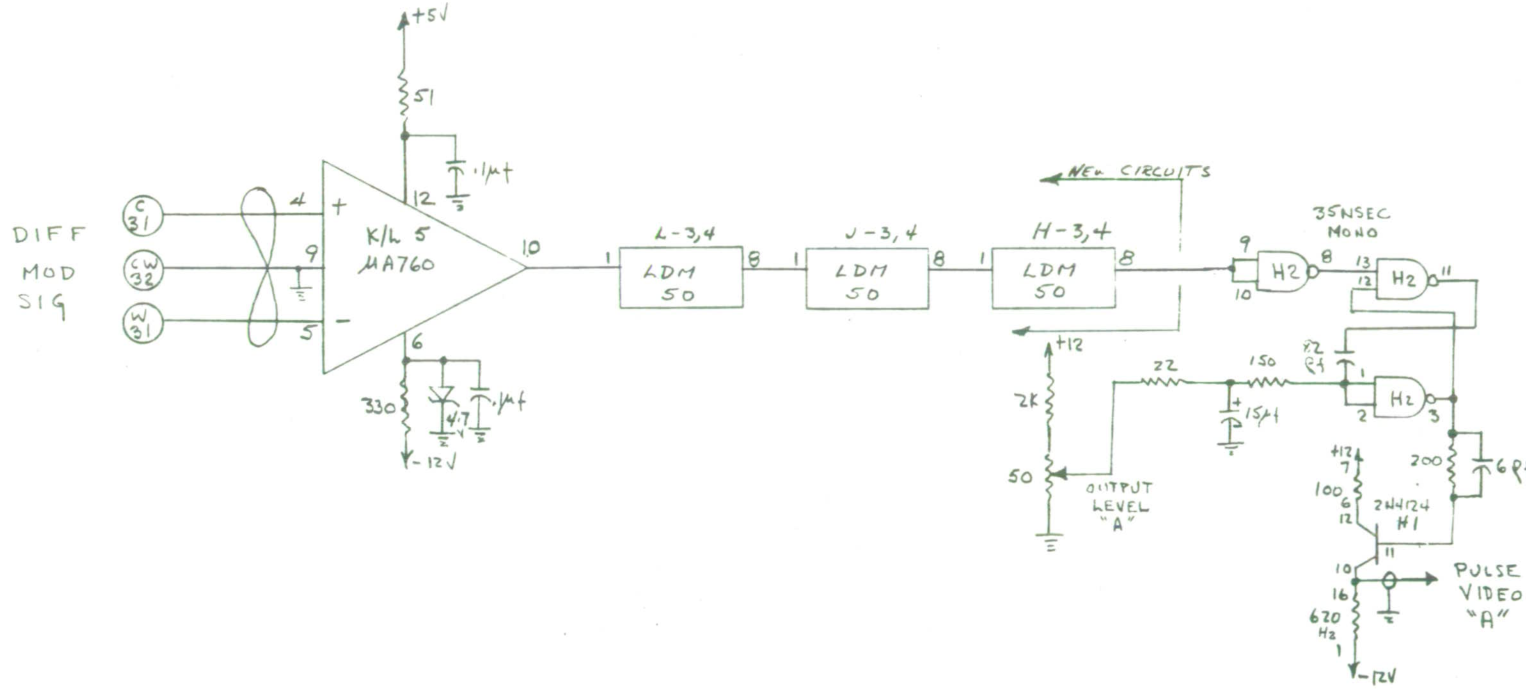


Fig. AII-18. "A" Channel Delay Equalizer (Sheet 1 of 3). Diff Board 1.

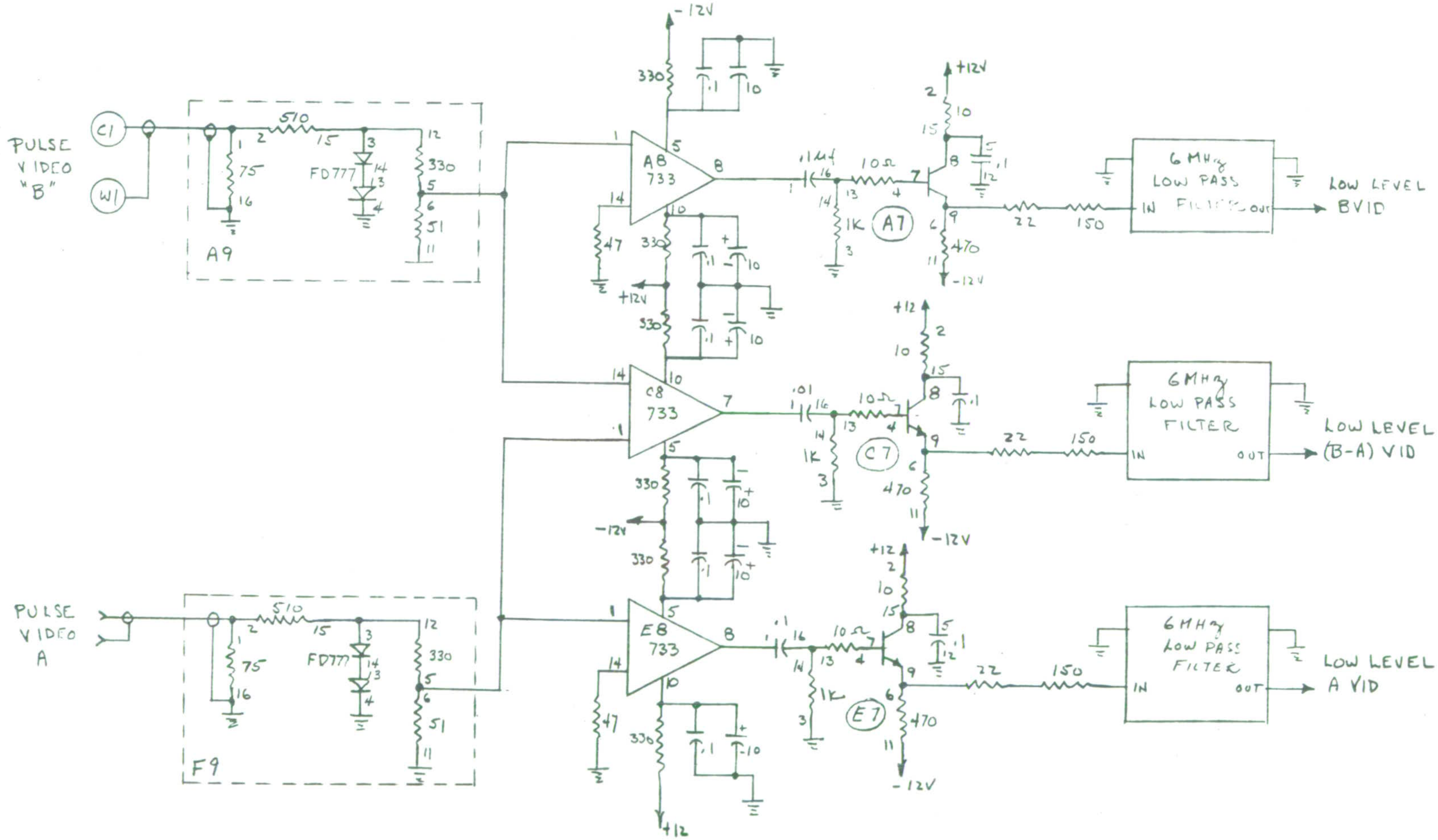


Fig. AII-19. Differencer Board Number 1 Pulse Video Integration (Sheet 2 of 3)

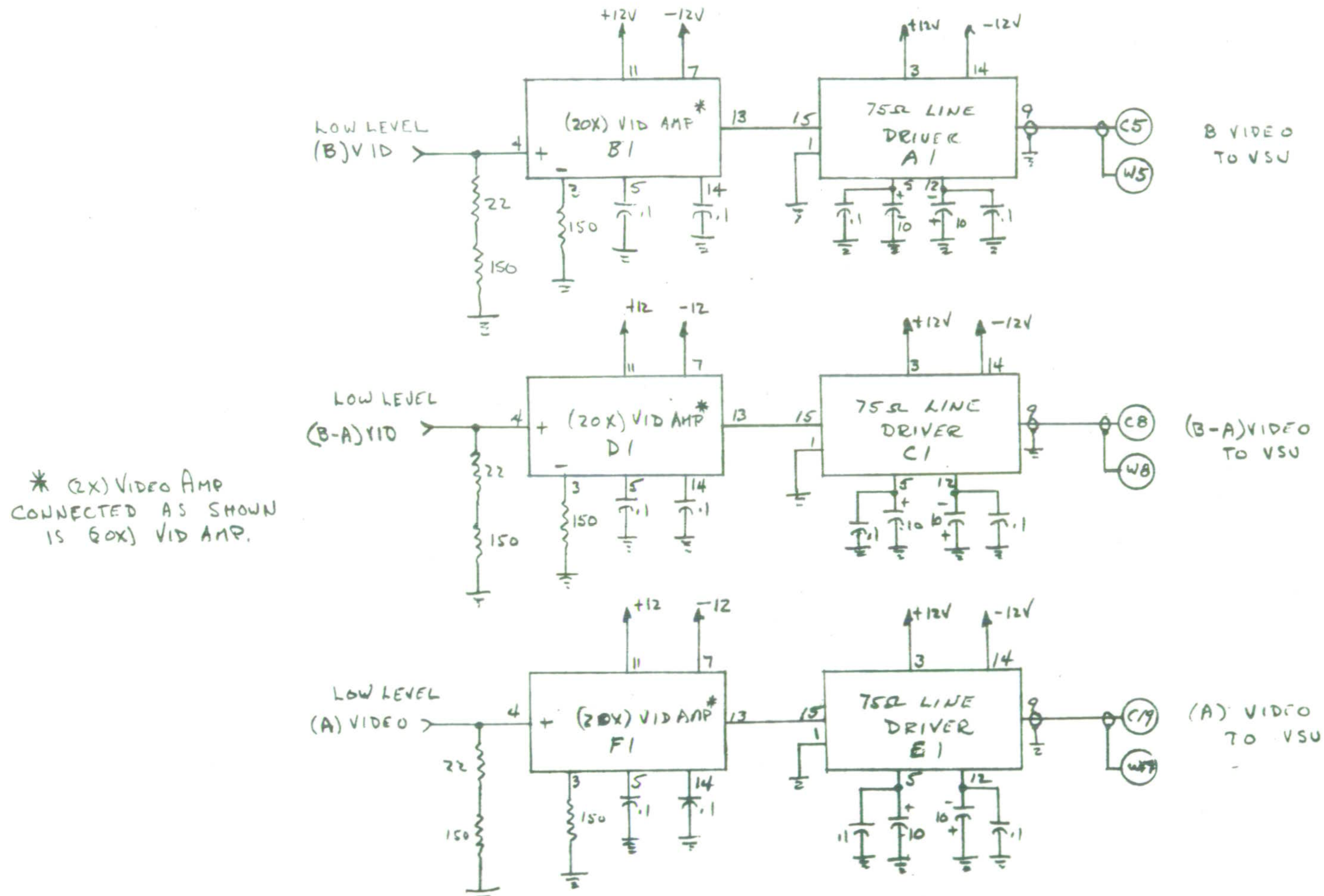
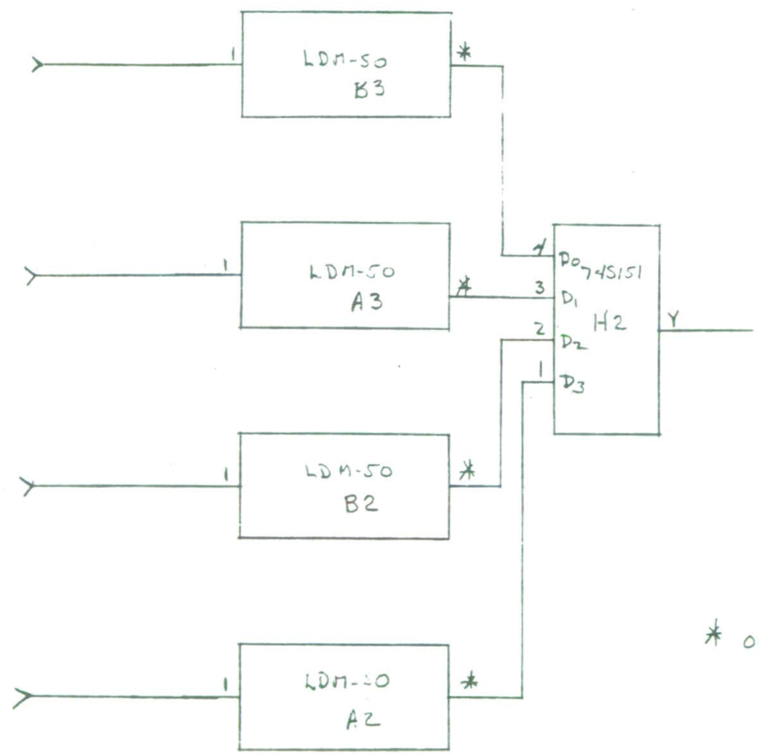


Fig. AII-20. Differencer Board Number 1 Video Amplifiers (Sheet 3 of 3).



PIN	DELAY USEC
1	0
12	10
4	20
10	30
6	40
8	50

ADD DELAY CKTS AS SHOWN

* OUTPUT TAP TO BE SELECTED ON TEST

Fig. AII-21. Differencer Board Number 2 Modification.

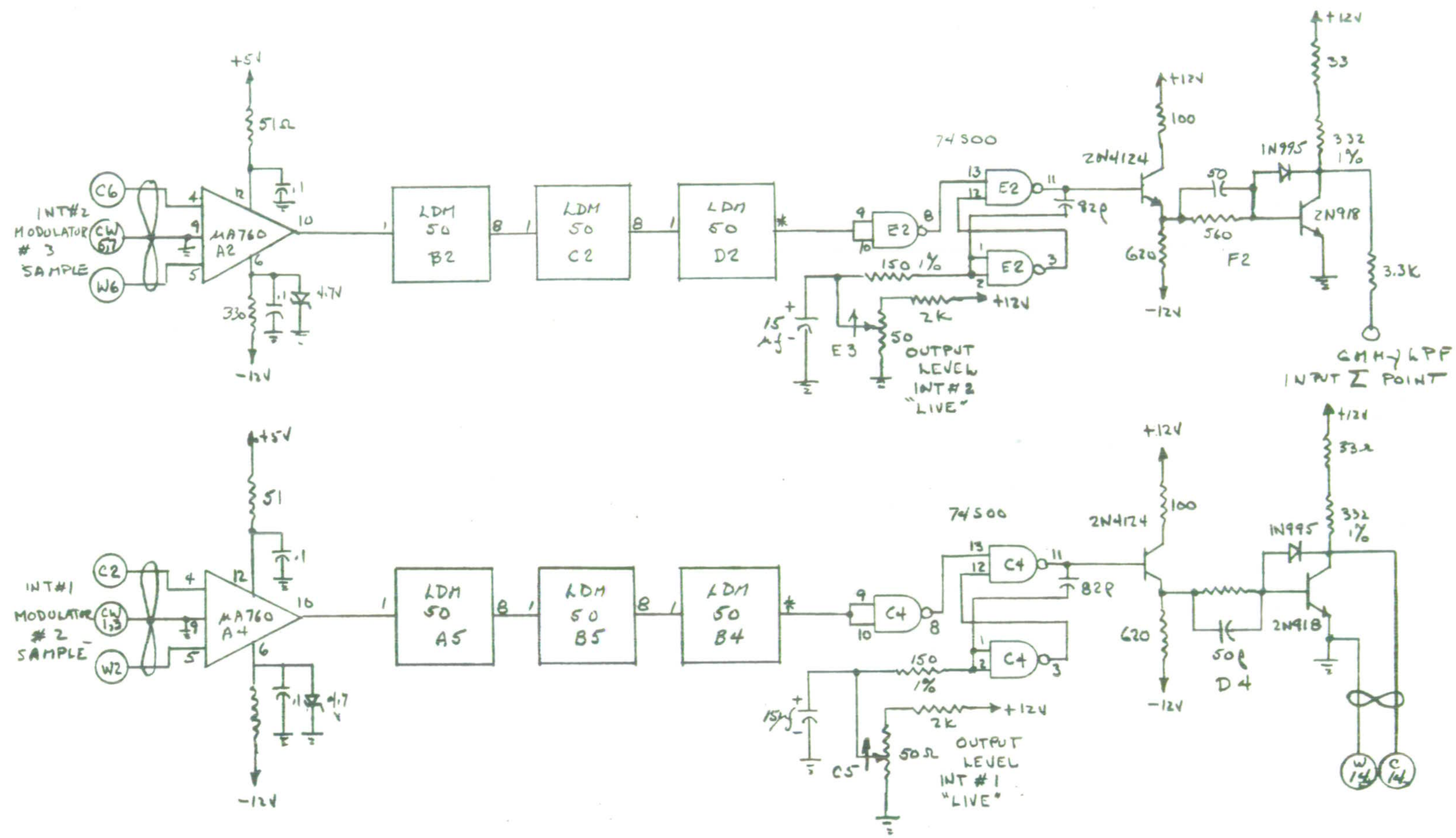


Fig. A11-22. Integrator Board Number 4 Modifications.

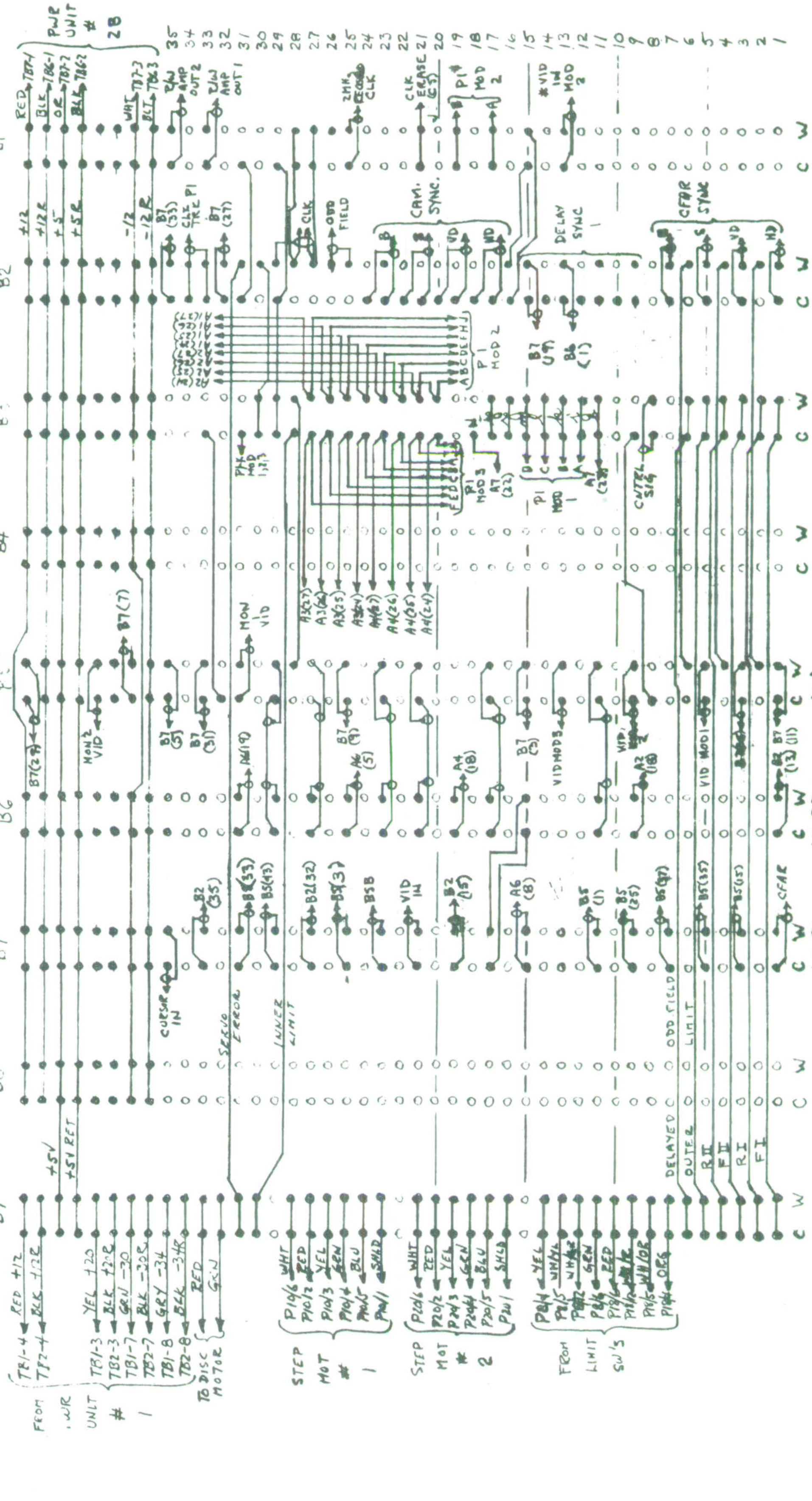


Fig. AII-23. Card Cage B Back Plane.

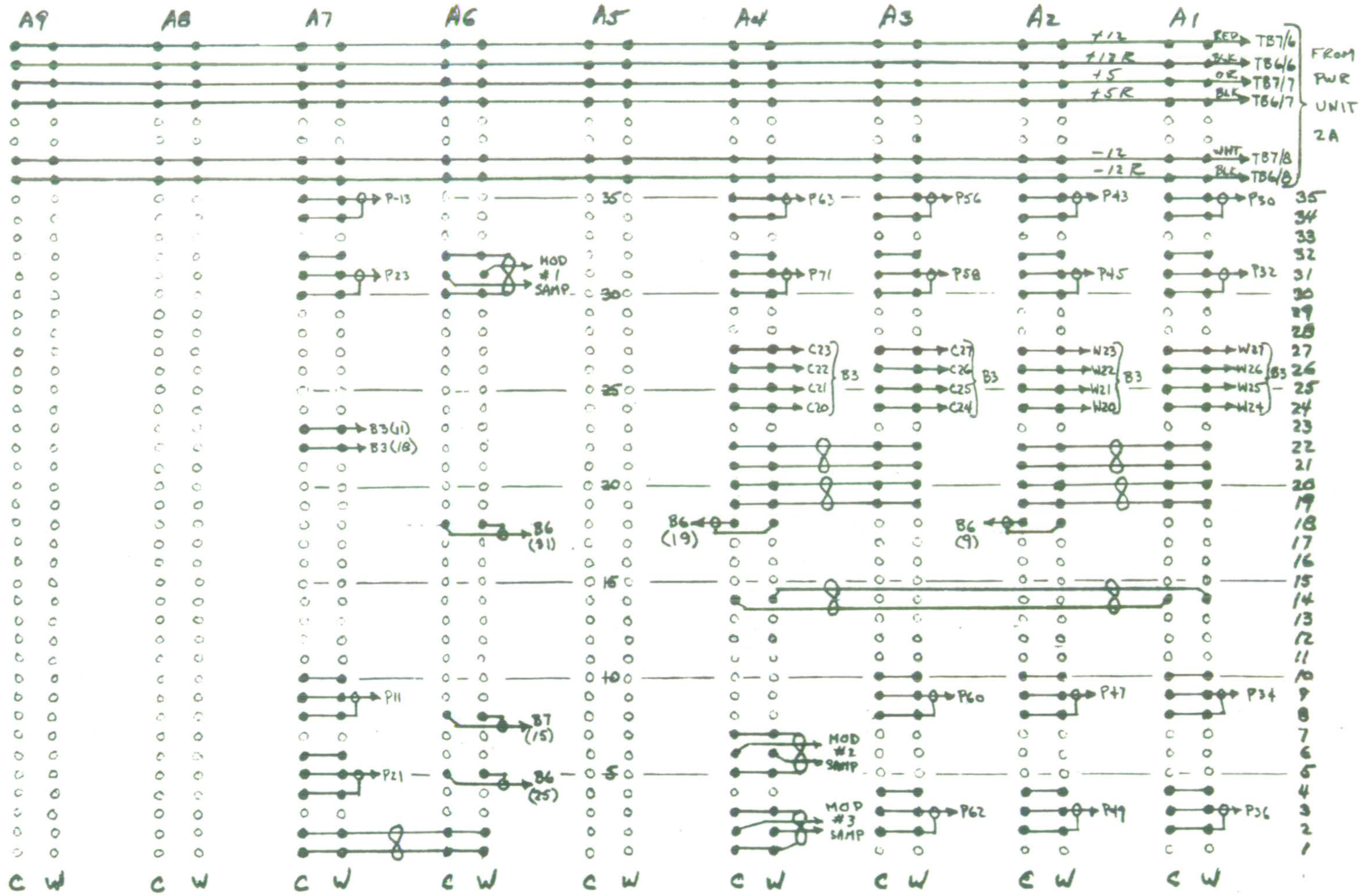


Fig. AII-24. Card Cage A Back Plane.

MOVIN HEAD ASSEMBLY #1 (TOP)
MODULATOR INTERCONNECTIONS

FROM HEAD	FUNCTION	TO MODULATOR #1
J8-1	DIFF-WE 1	J1-a
J8-2	DIFF-WE 2	J1-b
J5-C3	GND	P2-h
J5-W2	-12V	P2-d
J5-W3	+12V	P2-c
J5-W4	+5V	P2-a
J7-W6	FM INPUT #1	COAX (A) CENTER COND
J7-W5	FM INPUT #1	COAX (A) SHIELD
J6-W6	FM INPUT #2	COAX (B) CENTER COND
J6-W5	FM INPUT #2	COAX (B) SHIELD

MOVING HEAD ASS'Y #2 (BOTTOM)

FROM HEAD	FUNCTION	TO MODULATOR #1
J18-1	DIFF-WE-3	J1-c
J18-2	DIFF-WE-4	J1-d
J17-W6	FM INPUT #3	COAX (C) CENTER COND
J17-W5	FM INPUT #3	COAX (C) SHIELD
J16-W6	FM INPUT #4	COAX (D) CENTER COND
J16-W5	FM INPUT #4	COAX (D) SHIELD

Fig. AII-25.

FIXED HEAD ASSEMBLIES #1&#2 (BOTTOM)
MODULATOR INTERCONNECTIONS

FROM HEAD	FUNCTION	TO MODULATOR #2	
J28-C3	GND	P2-h	HARNESS #1
J28-W2	-12V	P2-d	
J28-W3	+12V	P2-c	
J28-W4	+5V	P2-a	
J29-1	INT#1 WE 1	J1-a	
-2	2	-b	
-3	3	-c	
-4	4	-d	
J42-1	5	-e	HARNESS #2
-2	6	-f	
-3	7	-h	
-4	8	-j	
J25-W6/W5	INT #1 FM INPUT # 1	COAX A	CENT/SHIELD HARNESS #1
J26-W6/W5	2	B	
J27-W6/W5	3	C	
J28-W6/W5	4	D	
J38 W6/W5	5	E	HARNESS #2
J39 W6/W5	6	F	
J40 W6/W5	7	H	
J41 W6/W5	8	J	

Fig. AII-26.

FIXED HEAD ASSEMBLIES #3 & #4 (TOP)
MODULATOR INTERCONNECTIONS

FROM HEAD	FUNCTION	TO MODULATOR #3	
J54-C3	GND	P2-h	HARNESS #1
J54-W2	-12V	P2-d	
J54-W3	+12V	P2-c	
J54-W4	+5V	P2-a	
J55-1	INT #2 WE 1	J1-a	
-2	2	-b	
-3	3	-c	
-4	4	-d	
J68-1	5	-e	HARNESS #2
-2	6	-f	
-3	7	-h	
-4	8	-j	
51-W6/W5	INT #2 FM INPUT # 1	COAX A	CENT/SHIELD HARNESS #1
J52-W6/W5	2	B	
J53-W6/W5	3	C	
J54-W6/W5	4	D	
J64-W6/W5	5	E	HARNESS #2
J65-W6/W5	6	F	
J66-W6/W5	7	H	
J67-W6/W5	8	J	

Fig. AII-27.

CLOCK TRACK WRITING MODULE (B-1)

[illegible]	FUNCTION	TO / FROM
C13/W13	H.DR. TO MODULATOR	COAX TO 1ST INT MODULATOR
C15/W15	H.DR. FROM SYNC. GEN.	(B2) C16/W16 TWISTED PAIR
CW 17	WRITE ENABLE #1	#22 WIRE TO 1ST INT MOD
C/W 19	WRITE ENABLE #2	#22 WIRE TO 1ST INT MOD
C/W 21	CLOCK CHAN. ERASE	#22 WIRE TO CLOCK R/W AMP (C5)
C25/W25	2MHz WRITE CLOCK	COAX TO CLOCK R/W AMP WRITE INPUT
W26/C29	ODD FIELD PULSE	(B2) W26/C29 TWISTED PAIR
W27/W28	2MHz FROM SYNC GEN	(B2) W27/W28 TWISTED PAIR
C31	H.DR. TO SYNC GEN	(B2) C31
C33/W33	R/W AMP #1 OUTPUT	COAX TO 1ST INT R/W AMP #1 OUTPUT
C35/W35	R/W AMP #2 OUTPUT	COAX TO 1ST INT R/W AMP #2 OUTPUT

Fig. AII-28.

Cycle Control Module (B-3)

N	Function	To/From
C/W 12	WE DIFF A (1)	DIFF MOD P1 A
C/W 13	WE DIFF B (2)	DIFF MOD P1 B
C/W 14	WE DIFF C (6)	DIFF MOD P1 C
C/W 15	WE DIFF D (5)	DIFF MOD P1 D
C 9	DIFF SEL	(B5) C8
W 20	INT#1 WE # 1	INT #1 MOD P1 A
W 21	" " 2	B
W 22	" " 3	C
W 23	" " 4	D
W 24	" " 5	E
W 25	" 6	F
W 26	" " 7	H
W 27	" 8	J
W28	DOUBLE /SINGLE INT	(B5) W28
C 22	INT#2 WE # 1	INT # 2 MOD P1 A
C 23	" " 2	" B
C 24	" " 3	" C
C 25	" 4	" D
C 26	" " 5	E
C 27	" " 6	" " F
C 20	" " 7	" " H
C 21	" " 8	" " J
C 31	DATA HOLD	DIFF P1-K; INT#1 P1-K; INT#2 P1K
C 33	REM SEL	(B5) C32

Fig. AII-29.

VIDEO SWITCHING UNIT MODULE B-5
BACK PLANE WIRING

PIN	FUNCTION	TO / FROM	
1	STRIP (B-A) VIDEO	(B7) C11/W11 COAX DOWN/UP	
3	STRIP INPUT VIDEO	(B7) C25/W25 COAX DOWN/UP	
5	VID TO DIFF MOD.	(A5) C12/W12 COAX UP	
C6	DIFF SEL	(B3) C9	
9	VID TO 1ST INT. MOD.	(A5) C16/W16 COAX UP	
11	INT #1 VID OUT	(B6)-C11/W11 COAX DIRECT	
13	VID TO 2ND INT. MOD.	(A5) C14/W14 COAX UP	
15	PROC VID OUT	(B-7)-C3/W3 COAX DOWN/UP	
17	INT #2 VID OUT	(B6)-C17/W17 COAX DIRECT	
W28	DOUBLE/SINGLE INT	(B3) W 28	
21	INT #2 VID TO MON 2	(B6) C21/W21 COAX DIRECT	
23	INT #1 VID TO MON 1	(B6) - C23/W23 COAX DIRECT	
25	(B-A) VID TO MON 1	(B7) - C9/W9) COAX DOWN/UP	
27	B VID TO MON 1	(B6) C27/W27 COAX DIRECT	
29	A VID TO MON 1	(B6) - C29/W29 COAX DIRECT	
31	MON #1 VID	BACK PANEL	
33	INPUT VID TO MON 1	(B7) - C31/W31 COAX UP/DN	
35	PROC VID TO MON 2	(B7) - C5/W5) COAX UP/DN	
37	(B-A) VID TO MON 2	(B7) - C7/W7 COAX UP/DN	*
39	MON #2 VID	BACK PANEL	*
41	+5 VOLTS	ALREADY CONNECTED	
43	INPUT VID TO MON 2	(B7) - C29/W29 COAX UP/DN	*
C32	REM SELECT	(B3) C33	
W2	DELAY A_0	(B2) W2	
W4	DELAY A_1	(B2) W4	
W6	DELAY A_2	(B2) W6	

WIRE B-5 TO B6 FIRST
B-5 TO B7 2ND
ALL OTHER B5 LAST

Fig. AII-30.

VIDEO PROCESSOR #2 MODULE B6

PIN	FUNCTION	TO / FROM
1	DELAYED SYNC #1	(B2) W13/C13 COAX DN/UP #
3		
5		
7		
9	INT#1 DEMOD OUT	(A-2) C18/W18 COAX UP
11	STRIP INT#1 VID	(B-5) C11/W11 COAX X
13		
15		
17	STRIP INT#2 VID	(B5) C17/W17 COAX X
19	INT#2 DEMOD OUT	(A-4) C18/W18 COAX
21	INT#2 VID TO MON 1	(B5) C21/W21 COAX X
23	INT#1 VID TO MON 1	(B5) C23/W23 COAX X
25	B-VID DEMOD OUT	(A6) C5/W5 COAX
27	B-VID TO MON 1	(B5) C27/W27 COAX X
29	A-VID TO MON 1	(B5) C29/W29 COAX X
31	A-VID DEMOD OUT	(A6) C19/W19 COAX UP
33		
35		
37	-12V	ALREADY WIRED
39		
41	+5V	ALREADY WIRED
43	+12V	ALREADY WIRED

INVERTED COAX
X PREVIOUSLY CALLED OUT

Fig. AII-31.

VIDEO PROCESSOR #1 MODULE B7

PIN	FUNCTION	TO / FROM	
1	PROC VID TO CFAR	BACK PANEL COAX	
3	PROC VID FROM VSU	(B5) C15/W15 COAX	X
5	PROC VID TO MON 2	(B5) C35/W35 COAX	X
7	(B-A) VIDEO TO MON 2	(B5) C37/W37 COAX	X
9	(B-A) VIDEO TO MON 1	(B5) C25/W25 COAX	X
11	(B-A) STRIP VID TO VSU	(B5) C1/W1 COAX	X
13			
15	(B-A) VID DEMOD OUT	(A6) C8/W8 COAX	UP
17	DELAYED SYNC #1	(B6) C15/W15 TWISTED PAIR	
19	DELAYED BLANK #1	(B2) W15/C15 COAX	#
21	SYSTEM VIDEO IN	BACK PANEL COAX	
23	STRIP VID TO BSB	BACK PANEL COAX	
25	STRIP VID TO VSU	(B5) C3/W3 COAX	X
27	C BLANK	(B2) W32/C32 COAX	#
29	INPUT VID TO MON 2	(B5) C43/W43 COAX	X
31	INPUT VID TO MON 1	(B5) C33/W33 COAX	X
33	C SYNC	(B2) W35/C35 COAX	UP/DN #
35	CURSOR IN	BACK PANEL COAX	
37	−12V	ALREADY WIRED	
39			
41	+5V	ALREADY WIRED	
43	+12V	ALREADY WIRED	

\# REVERSE COAX

X ALREADY CALLED OUT

Fig. AII-32.

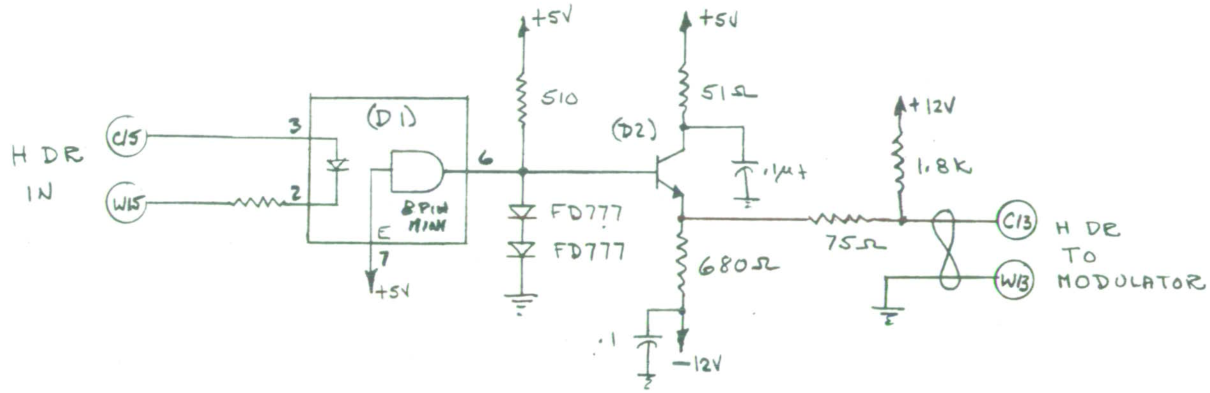
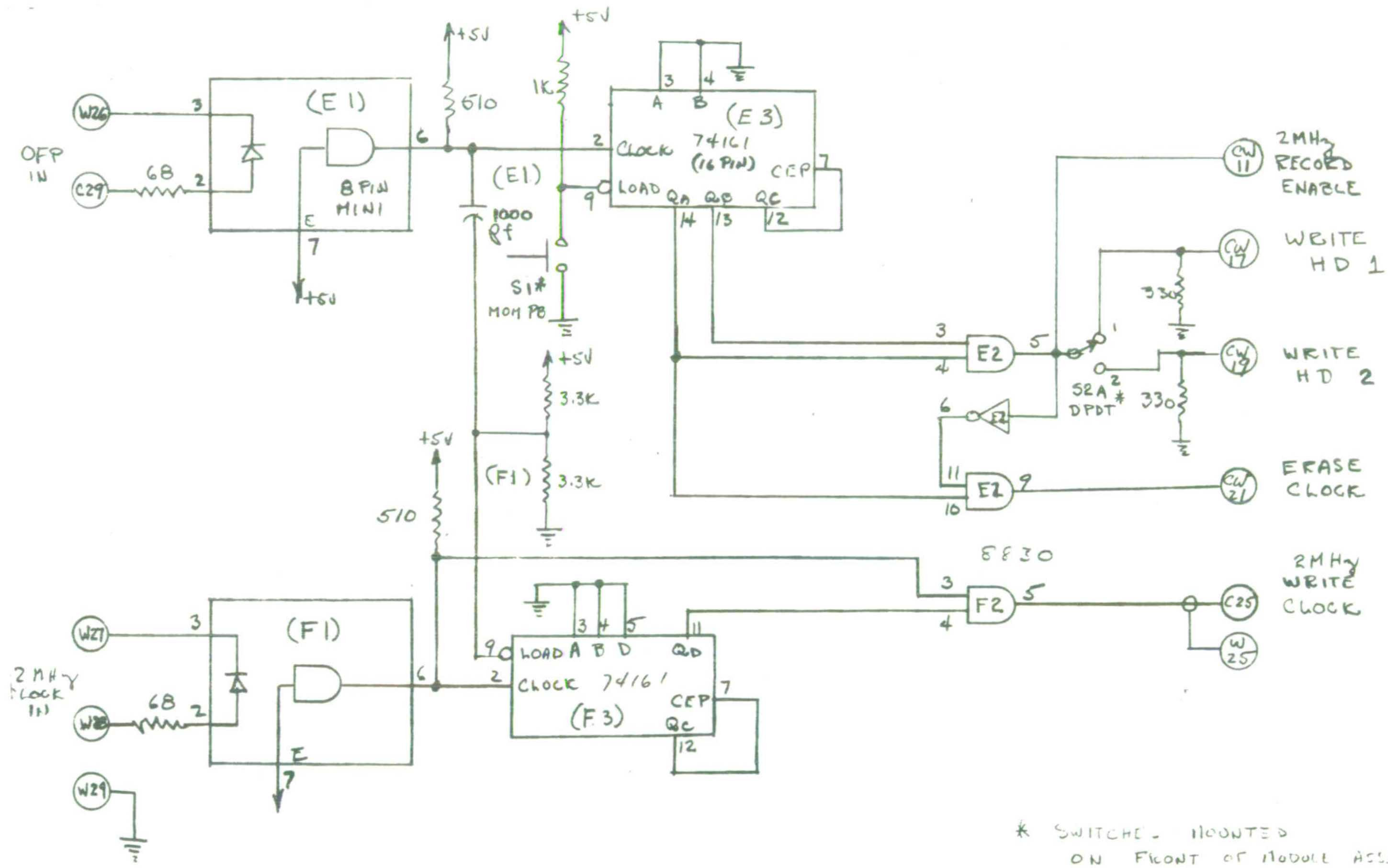


Fig. AII-33. Clock Track Writing (Sheet 1 of 3).



* SWITCHES MOUNTED ON FRONT OF MODULE ASSEMBLY

Fig. AII-34. Clock Track Writing (Sheet 2 of 3) Write Enable & Gapped Clock.

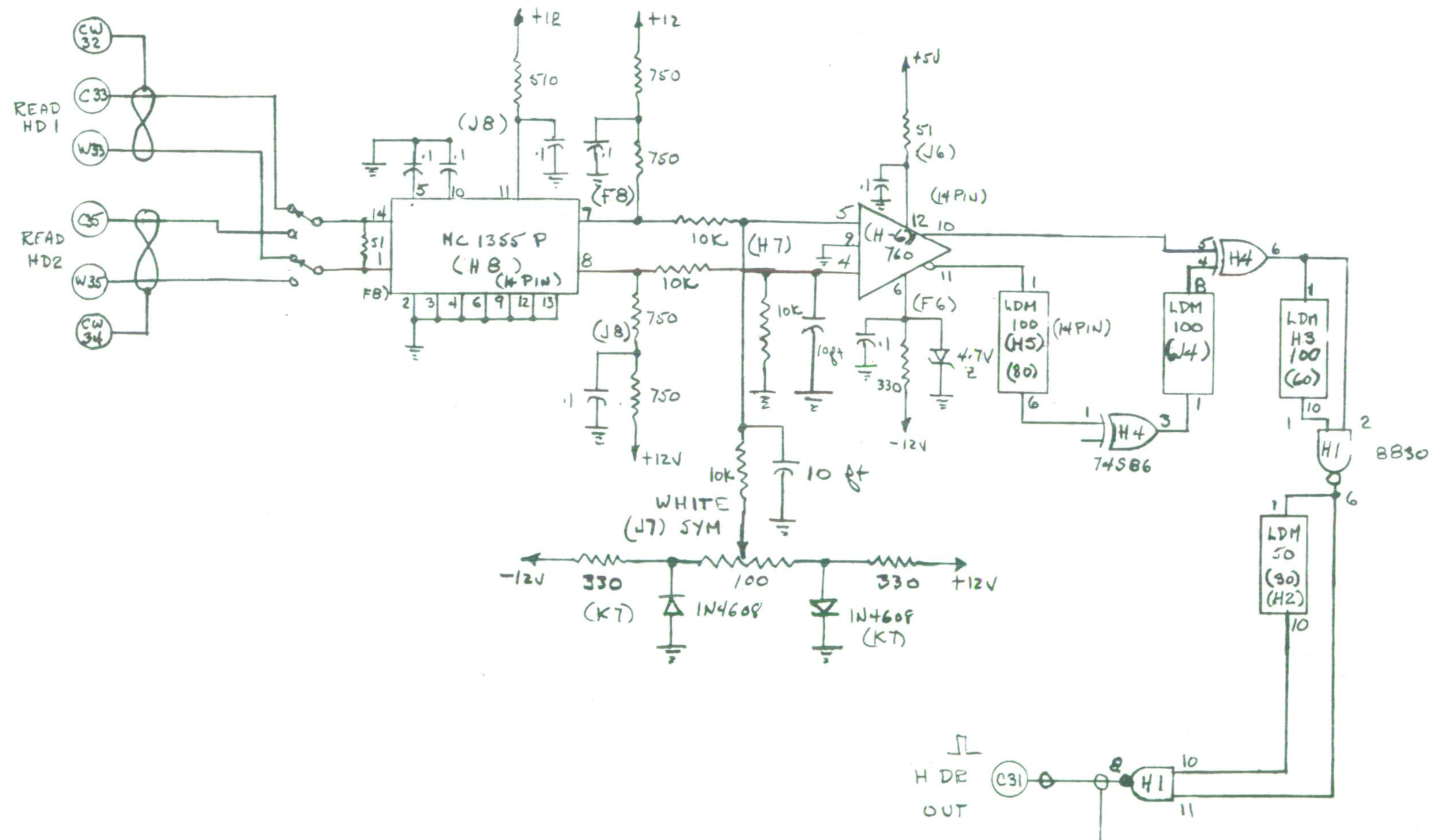
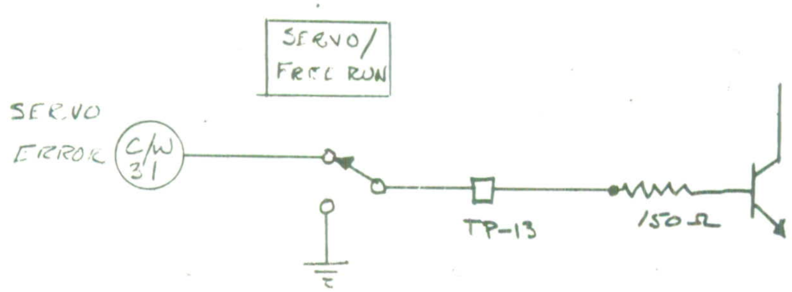
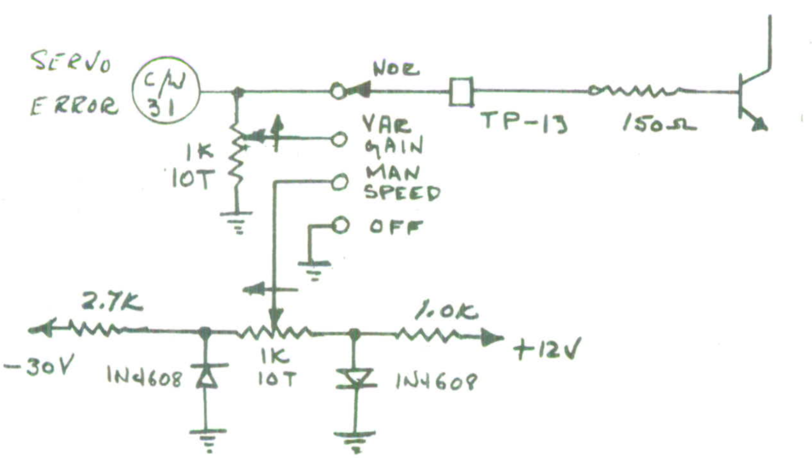


Fig. A11-35. Clock Track Writing (Sheet 3 of 3) H-Dr. Demod.

SERVO MOTOR DRIVER MODIFICATIONS



ORIGINAL CIRCUIT



MODIFIED FOR CLOCK TRACK WRITING

Fig. AII-36.

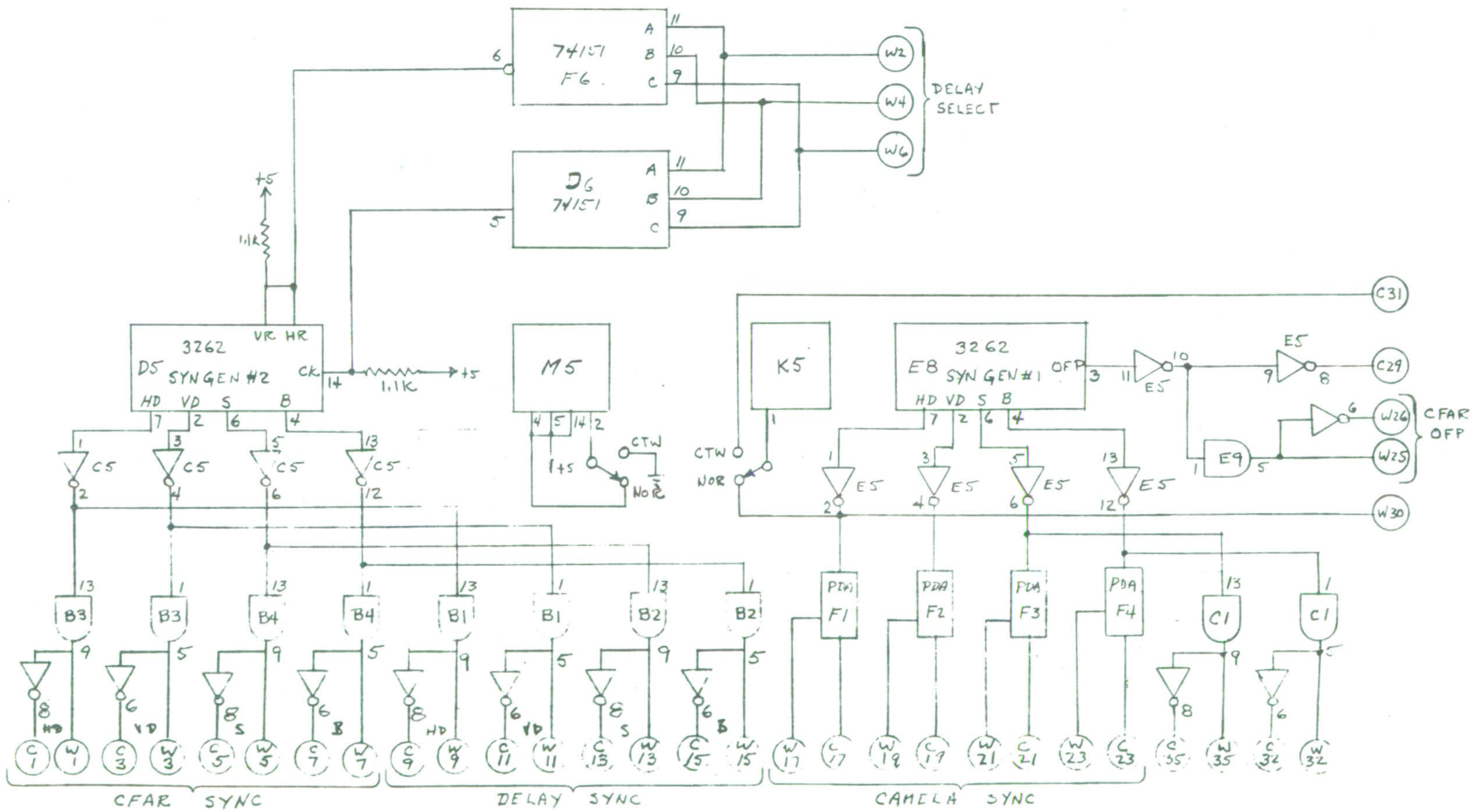


Fig. AII-37. Servo & Sync Gen (B2) Modifications.

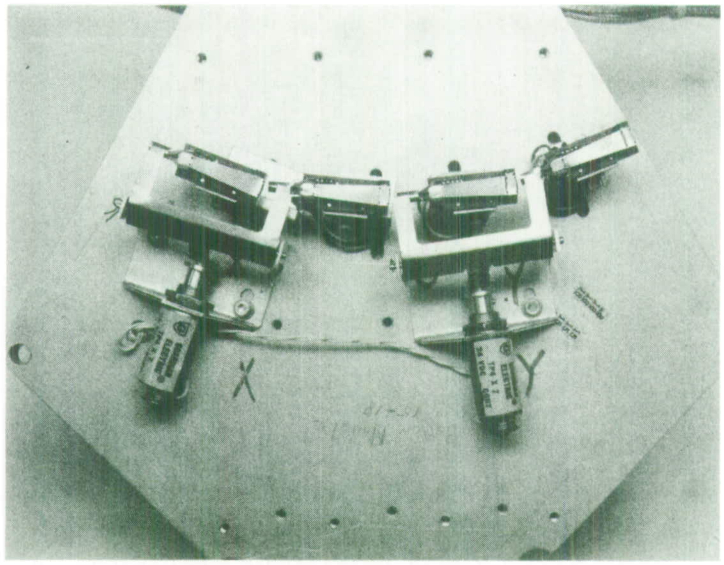


Fig. AII-38. Fixed Heads With Lifters Installed.

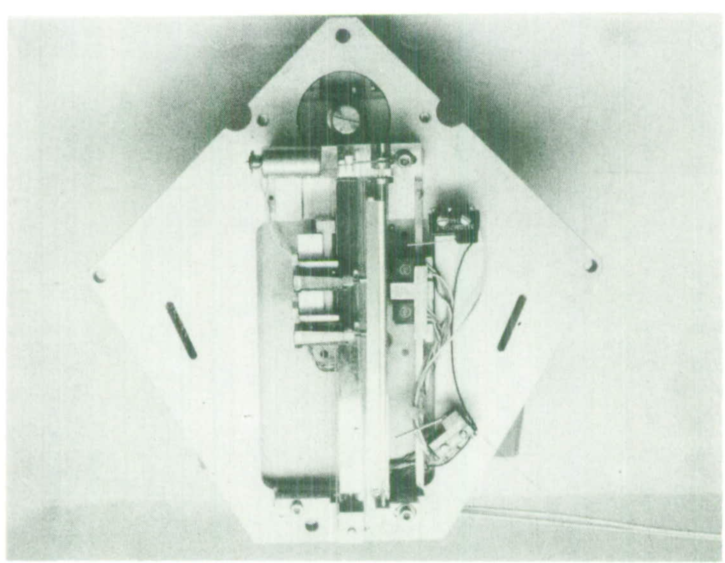


Fig. AII-39. Moving Heads With Lifters Installed.

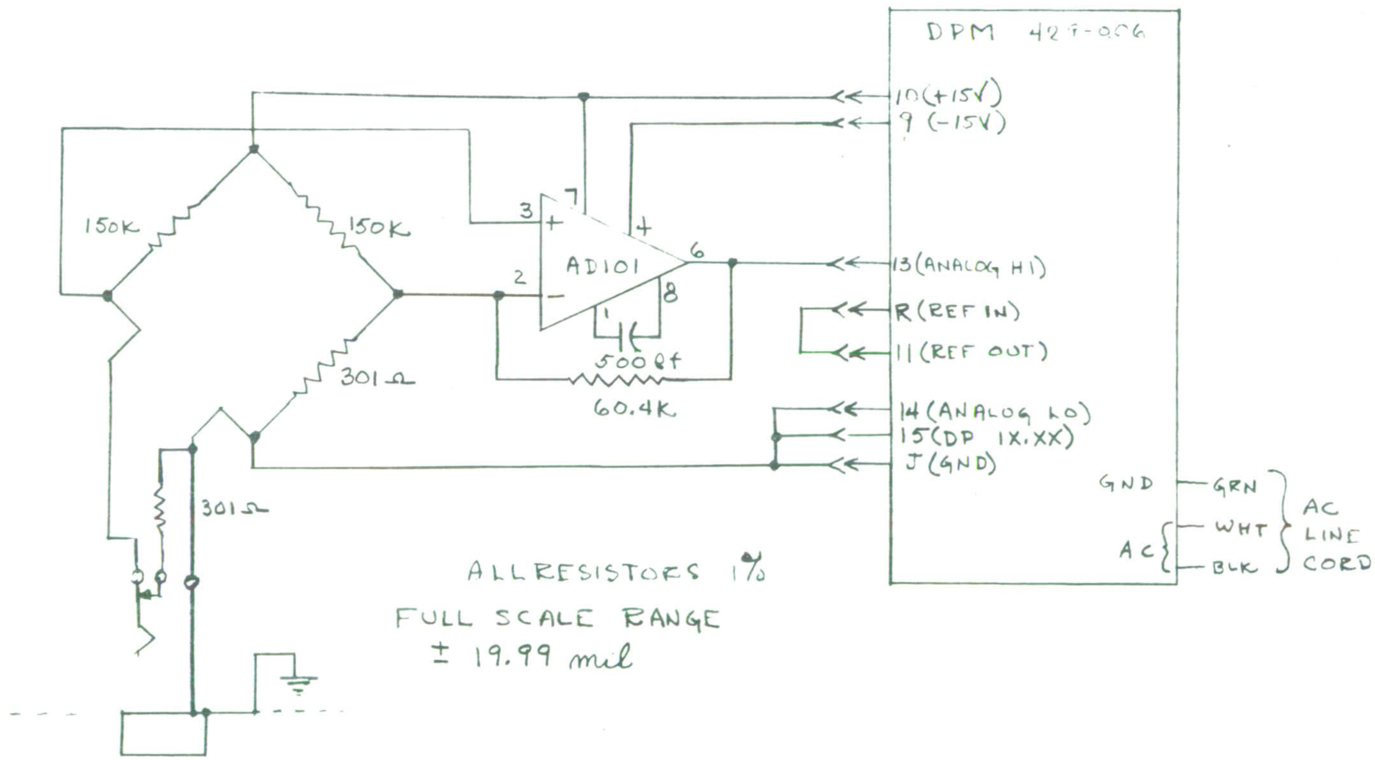


Fig. AII-40. Unimeasure 80 readout.

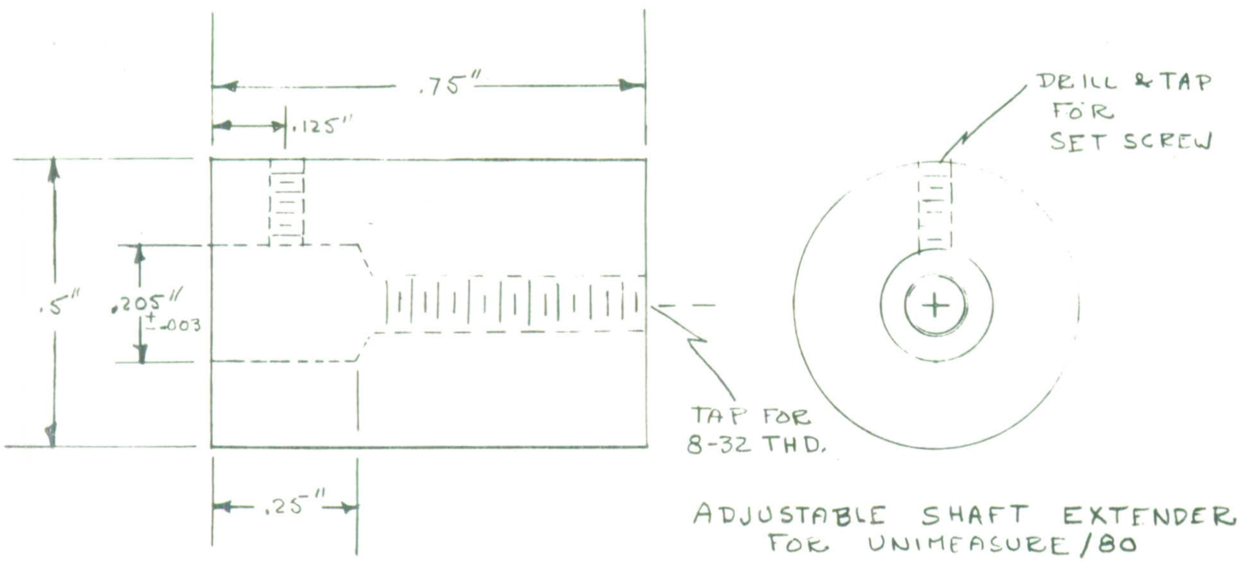

.75"
.125"
.5"
.205"
± .003
.25"
DRILL & TAP
FOR
SET SCREW
TAP FOR
8-32 THD.
ADJUSTABLE SHAFT EXTENDER
FOR UNIMEASURE/80

Fig. AII-41.

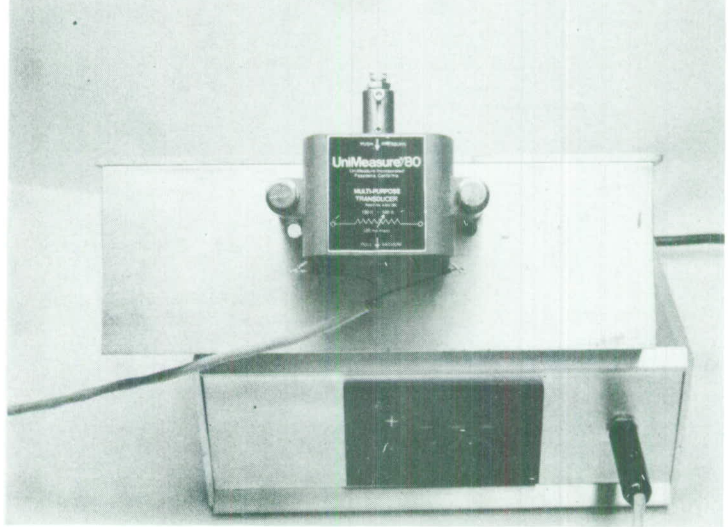


Fig. AII-42

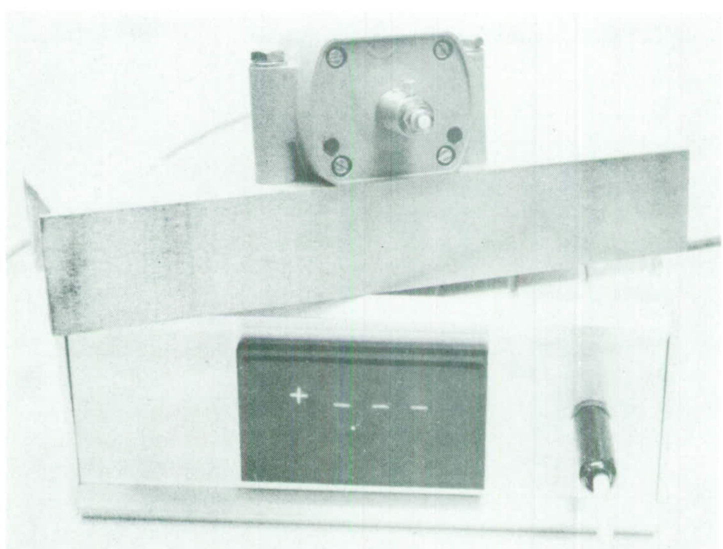


Fig. AII-43

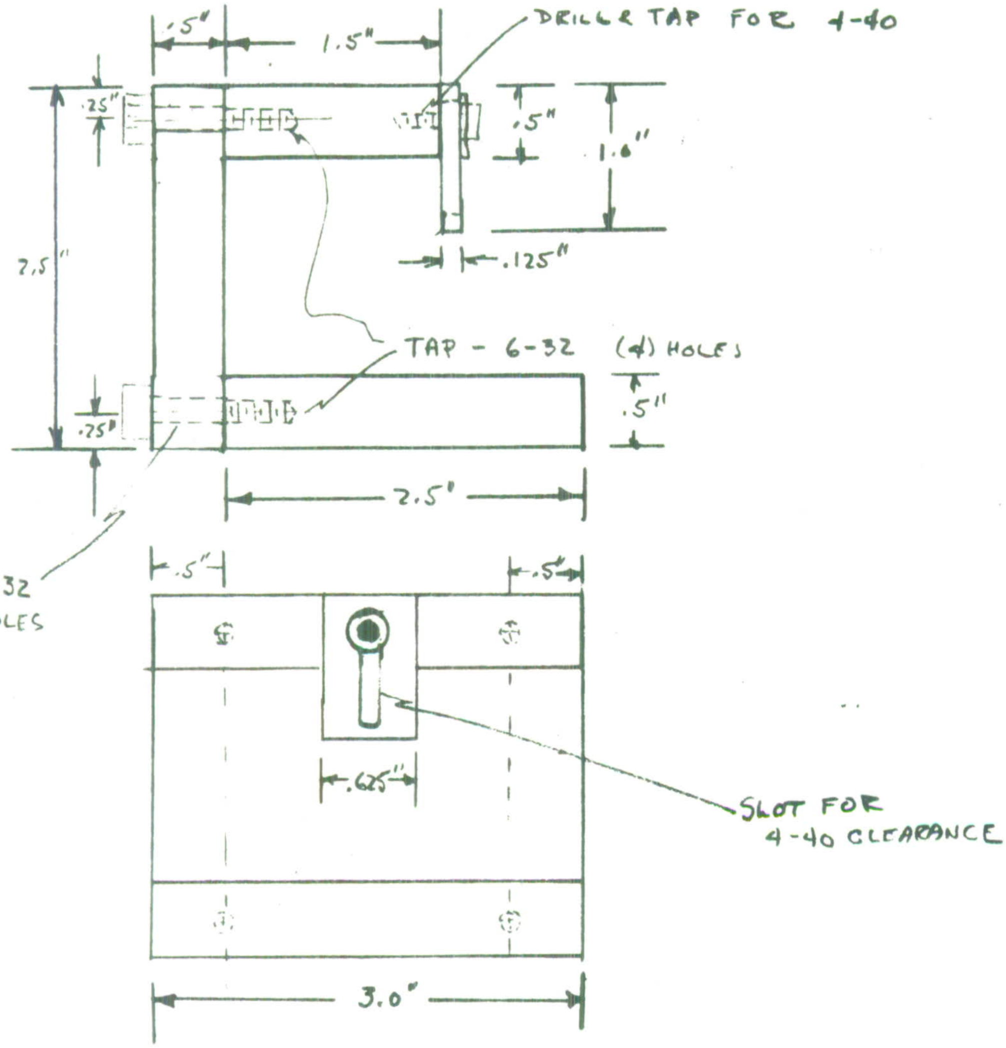


Fig. AII-44. Head height adjust jig.

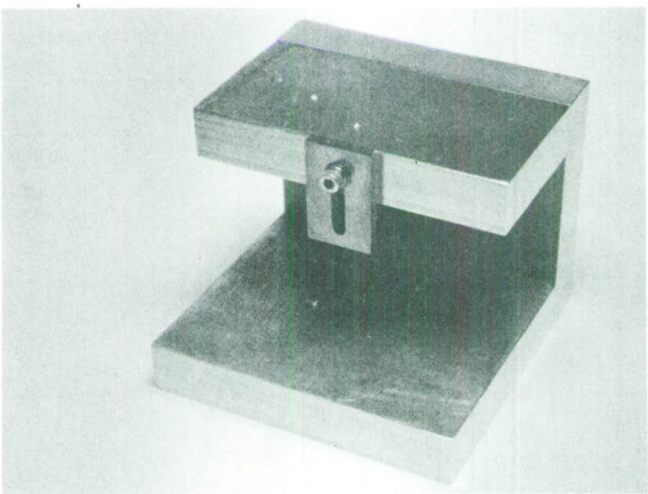


Fig. AII-45

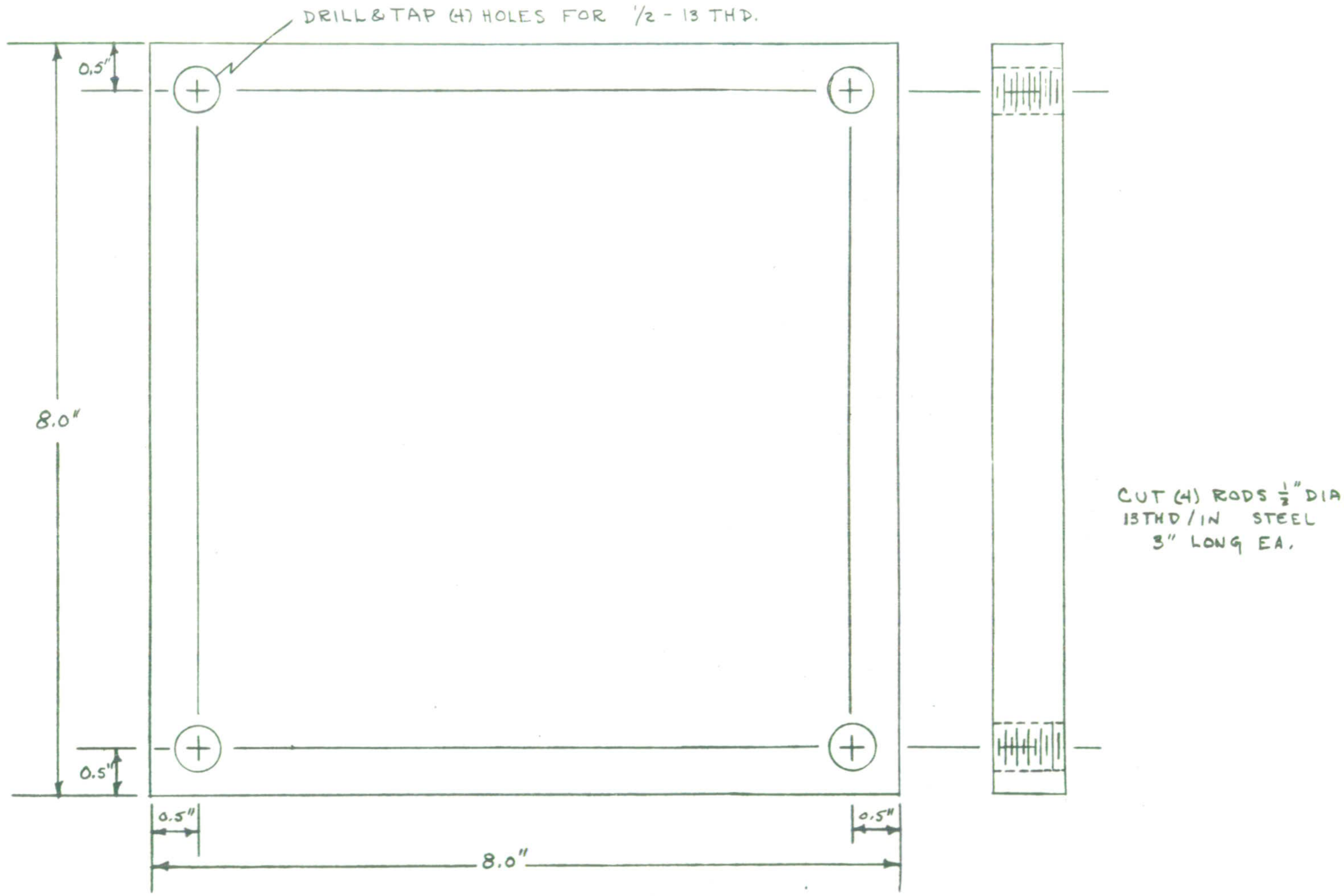


Fig. AII-47. Head Alignment Jig Bottom Plate Make (1) From 3/4" Alum.

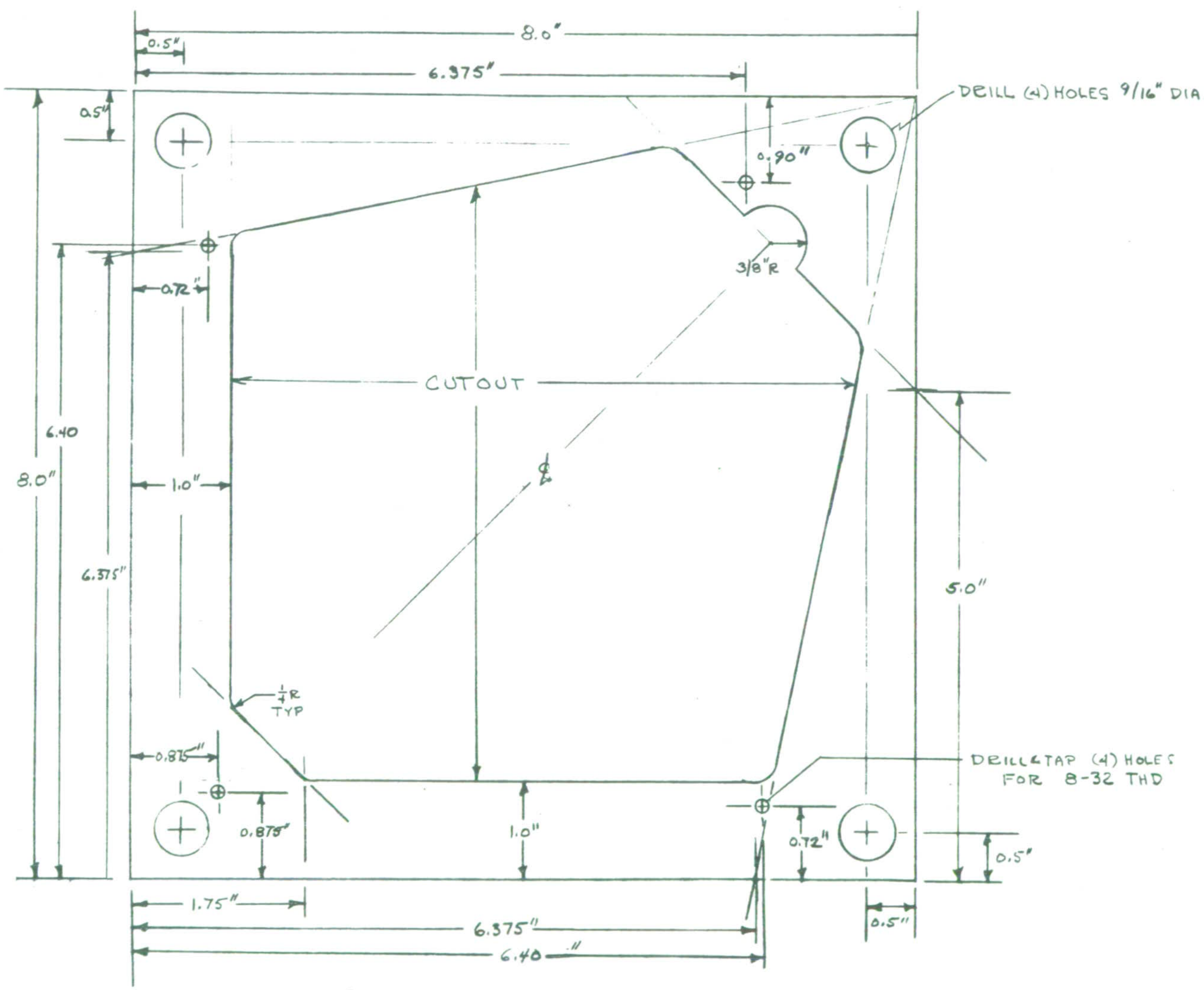


Fig. A11-46. Head Alignment Jig Make (1) From 3/8" Alum.

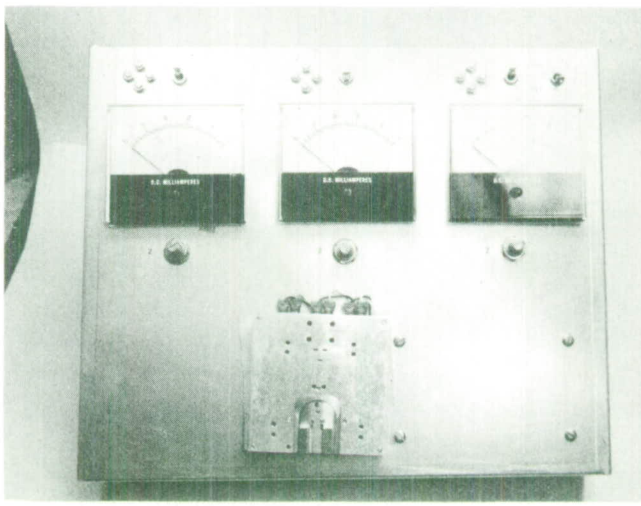


Fig. AII-48.

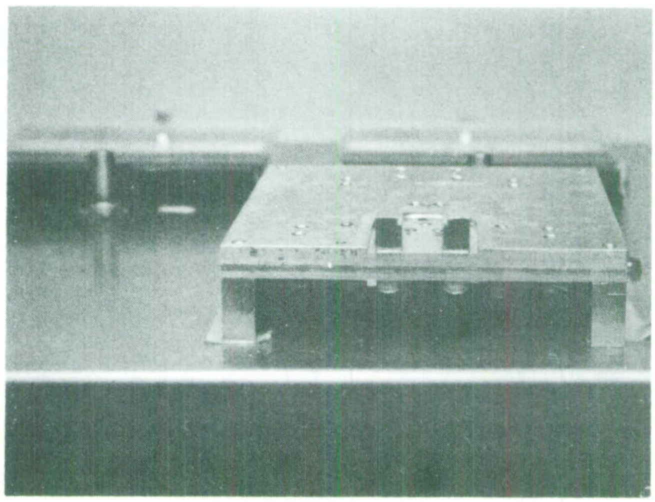


Fig. AII-49

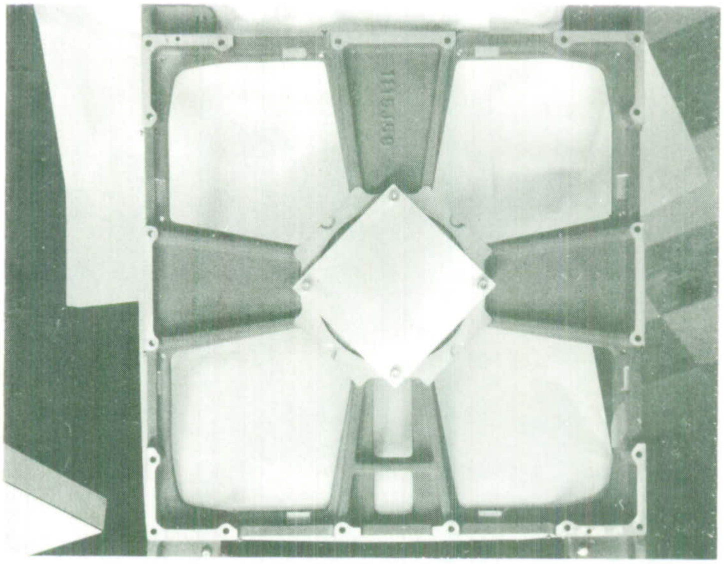


Fig. AII-50.

Fig. AII-51

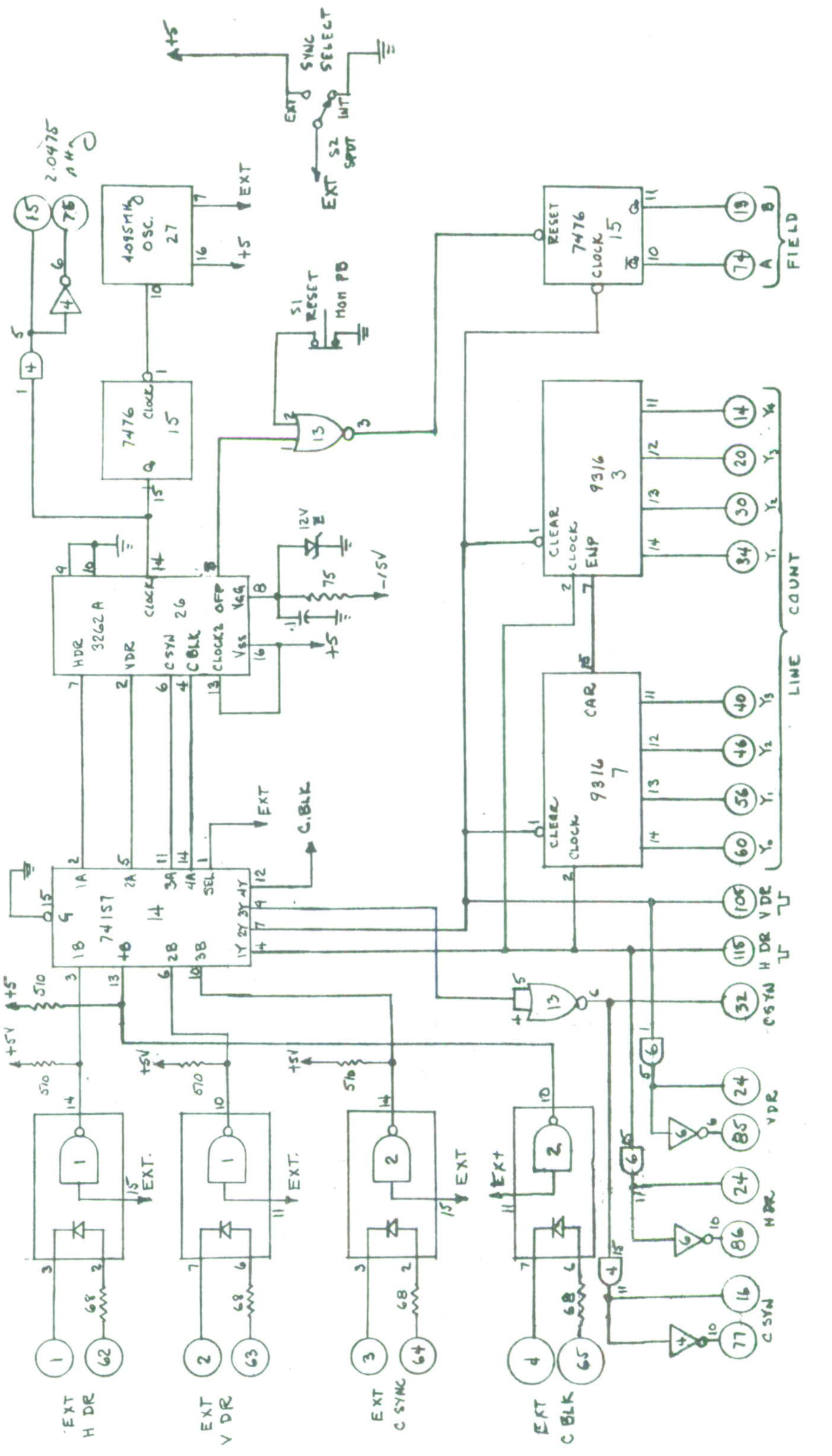


Fig. AIII-1. Simulator Board 2 Sync (Sheet 1 of 2).

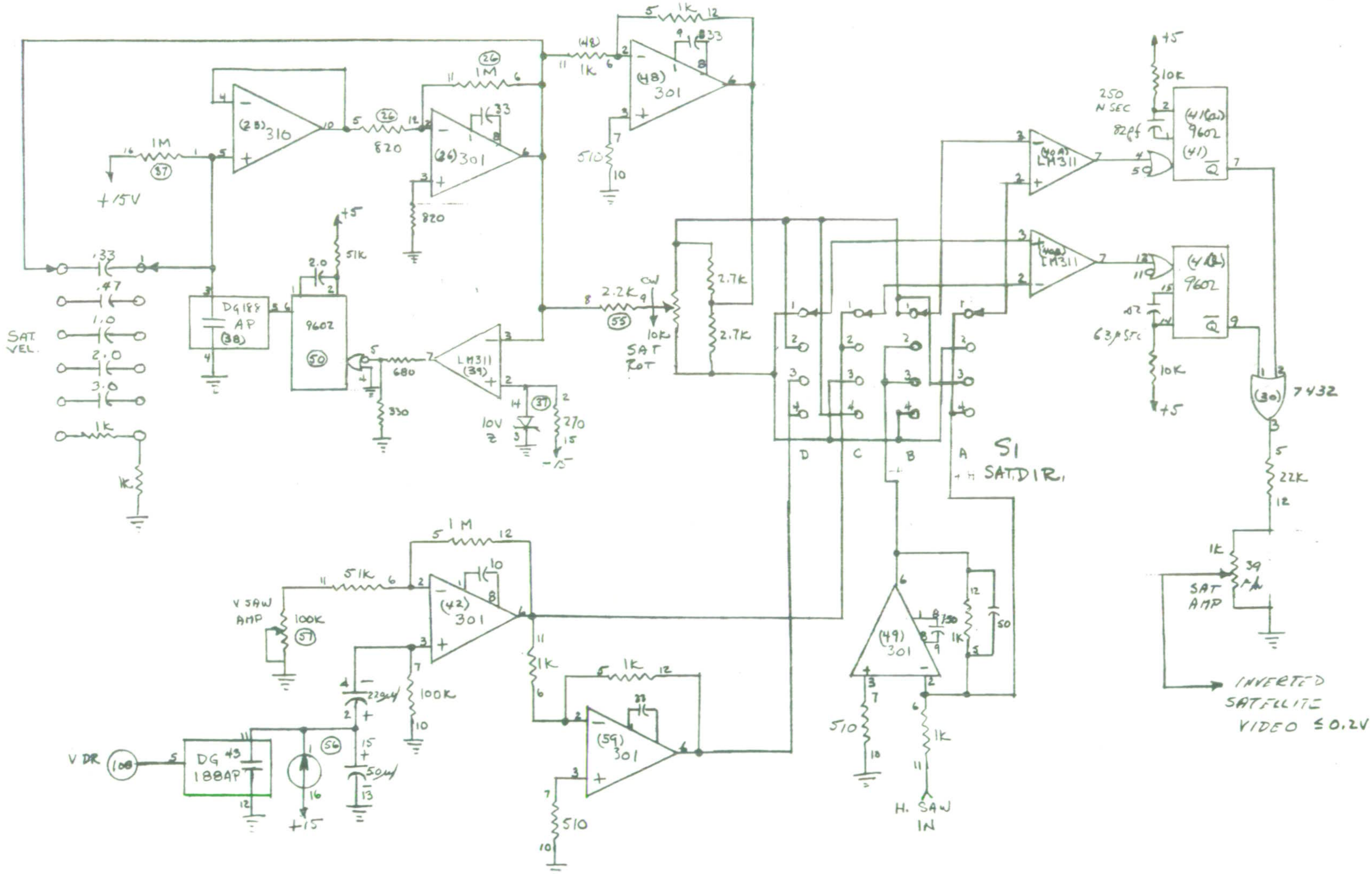


Fig. AIII-2. Simulator Board 1 Satellite Generator.

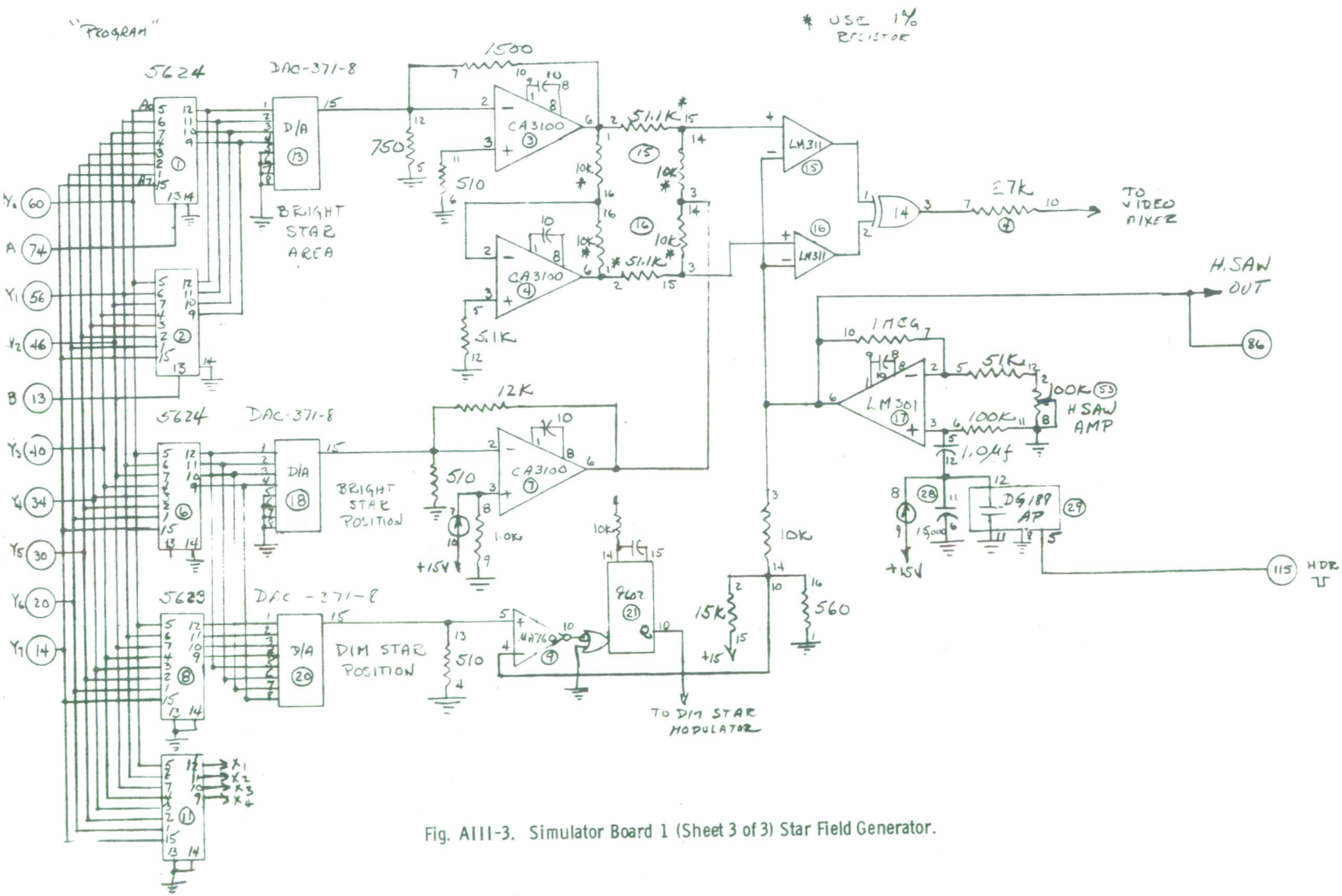


Fig. AIII-3. Simulator Board 1 (Sheet 3 of 3) Star Field Generator.

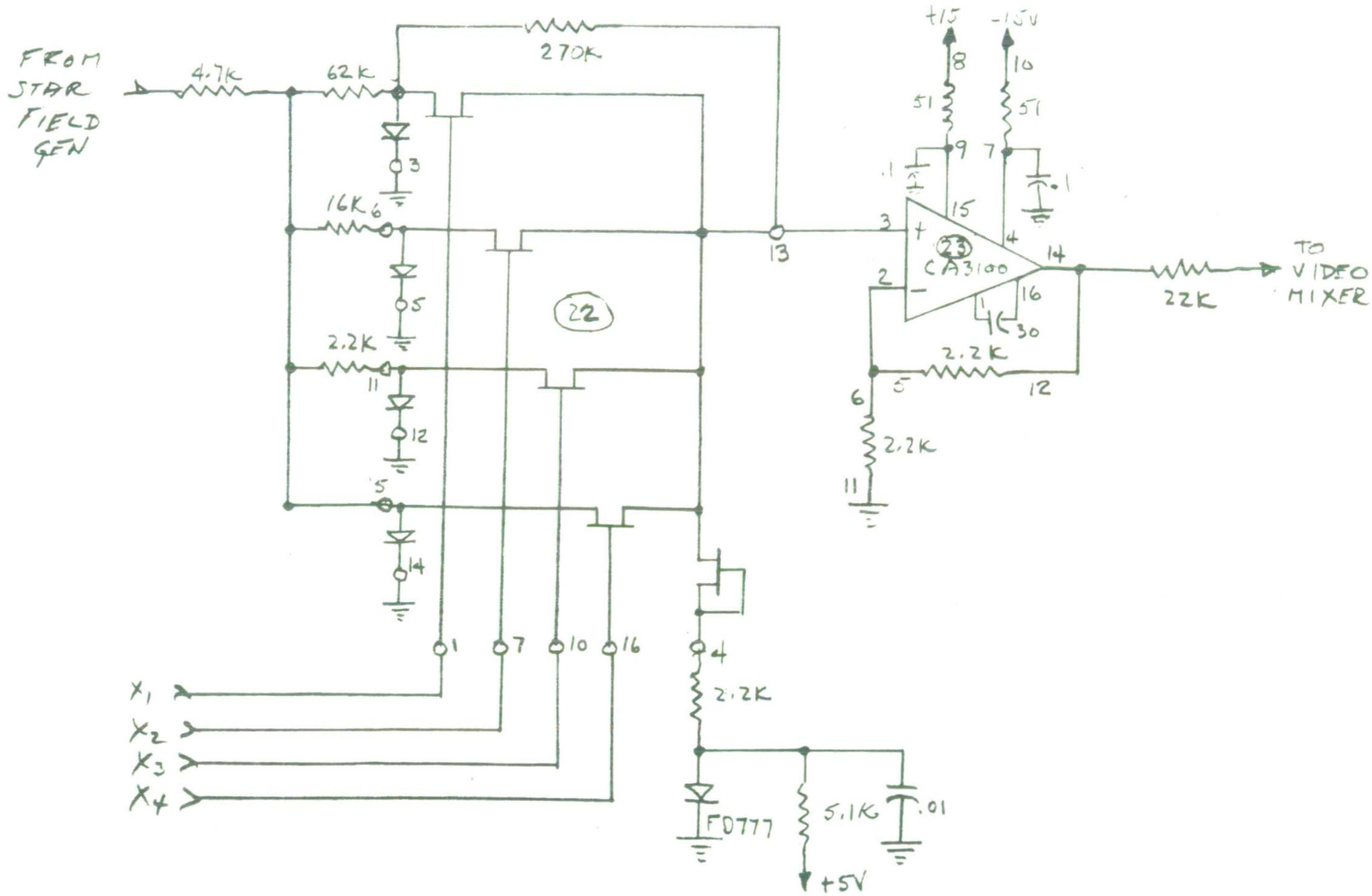


Fig. AIII-4. Dim star amplitude modulator.

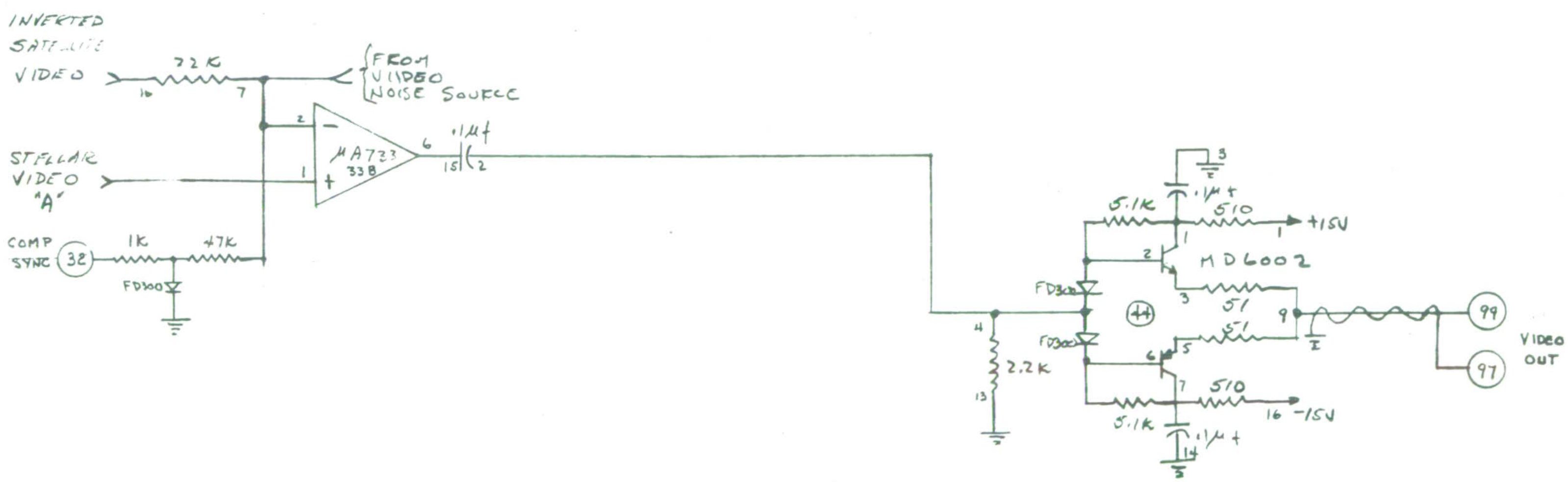


Fig. AIII-5. Simulator Board 1 Video Mixing.

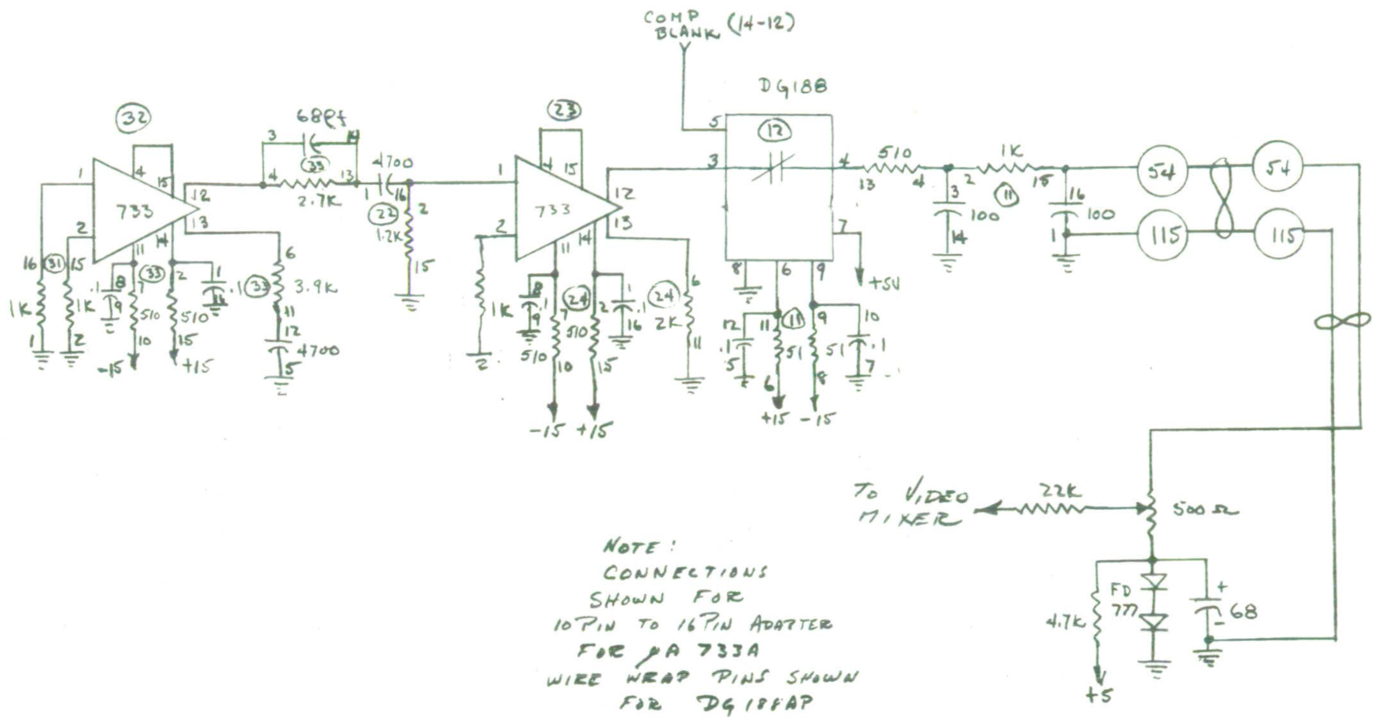


Fig. AIII-6. Video Noise Source Simulator Board 2 (Sheet 2 of 2)

FROM PINS		VIDEO SIMULATOR FROM MOD 3 TO	M/P	SYNC GENERATOR FROM MOD 5 TO	M/P	FROM MOD TO M/P	±15 VOLT SUPPLY FROM MOD 13 TO	M/P	±5 VOLT SUPPLY FROM MOD 25 TO	M/P
1	62			H DR ϕ	H DR R					
2	63			V DR ϕ	VDR R					
3	64			SYNC ϕ	SYNC R					
4	65									
5	66									
6	67									
7	68									
8	69	+5V		+5V					+5V	+5V
9	70									
10	71									
11	72	-15V					-15V	-15V		
12	73									
13	74	5-13	5-74	∞	∞					
14	75	5-14		∞						
15	76	+15V					+15V	+15V		
16	77									
17	78									
18	79	+5R		+5R			±15VR	±15VR	±5VR	±5VR
19	80									
20	81	5-20		∞						
21	82									
22	83									
23	84									
24	85									
25	86									
26	87									
27	88	9		9						
28	89									
29	90									
30	91	5-30		∞						
31	92									
32	93	5-32		∞						
33	94									
34	95	5-34		∞						
35	96									
36	97	18	ϕ LIVE VID R	18						
37	98		DELAY OUT							
38	99		ϕ LIVE VID							
39	100	-5V							-5V	-5V
40	101	5-40		∞						
41	102									
42	103									
43	104									
44	105									
45	106	27		27						
46	107	5-46		∞						
47	108		5-108		∞					
48	109		ϕ DIFF VID R							
49	110									
50	111		ϕ DIFF VID							
51	112									
52	113									
53	114		DELAY IN							
54	115	36	5-115	36	∞					
55	116						AC	AC	AC	AC
56	117	5-56		∞						
57	118									
58	119						ACR	ACR	ACR	ACR
59	120									
60	121	5-60		∞						
61	122									

Fig. AIII-7. Simulator Nest Wiring.

ACKNOWLEDGEMENT

The author wishes to acknowledge the cooperation of all his colleagues in Group 94, Space Surveillance, in this project, particularly:

Ms. Irene Coates who performed all the hard work of wiring the circuits and assembling the components with diligence and dedication; and,

Mr. Norman Pong who assisted in the final testing and debugging and offered many helpful suggestions.

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		6. PERFORMING ORG. REPORT NUMBER Technical Note 1977-32
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artificial satellites
electro optical MTI system
satellite detection
video disc recorder
GEODSS

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes an electro-optical moving target indicator (MTI) system that was developed for the detection of satellites in deep space. The system operates on standard RS-170 video provided from a telescope mounted TV camera. The principle of operation is to remove stationary clutter background (stars), enhance signal to noise by integration of successive frames and provide automatic detection by means of constant false alarm rate (CFAR) thresholding in combination with majority logic correlation. A detailed description of the theory of operation as well as complete design details are given along with actual field test results.

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